MODULE – 01

~~UNIT – 01~~

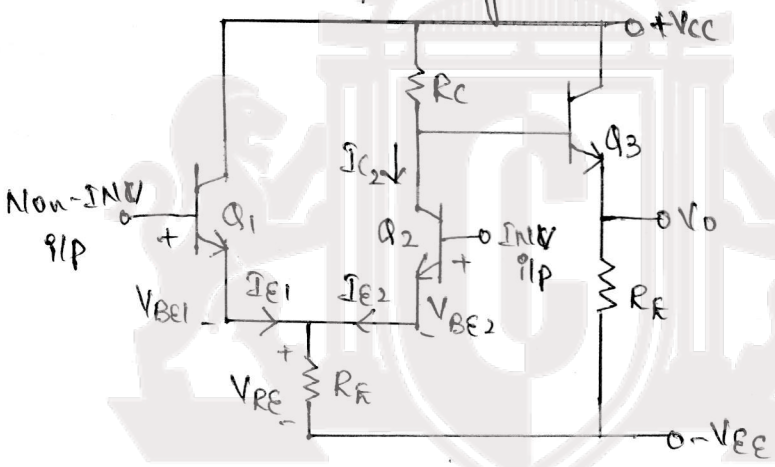
Assignment Questions with Solutions

SUB: LINEAR INTEGRETED CIRCUITS AND IT'S APPLICATIONS

1. → What is an op-amp? Explain the working of its basic circuit
→ Explain the basic circuit of operational amplifier.
→ With a neat circuit diagram, Explain the basic op-amp ckt.

→ An operational amplifier is a high gain differential amplifier circuit with two i/p terminals (INV or NON INV) and one o/p terminal.

→ Basic CKT consists of a differential amplifier as i/p stage and emitter follower as o/p stage shown in fig 1.



→ The differential amplifier produces a vtg change at the collector of Q_2 when a difference i/p vtg applied to the bases of Q_1 and Q_2. Q_3 is emitter follower to produce low input impedence.

→ Assume $V_{CC} = 10V$, $V_{EE} = -10V$, $R_E = 4.7k\Omega$, $R_C = 6.8k\Omega$ & $V_{BE} = 0.7V$

→ Case 1: when two i/p terminals are grounded.

Let Q_1 and Q_2 are matched transistors i.e, $V_{BE1} = V_{BE2}$ and $\beta_1 = \beta_2$

$I_{E1} = I_{E2}$ and flows through common R_E

$$\because I_E = I_{E1} + I_{E2} = \frac{V_{RE}}{R_E} \quad -(1)$$

Q_1 & Q_2 bases are grounded, $V_{RE} = V_{EE} - V_{BE}$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{R_E} \quad -(2)$$

$$\text{and } V_0 = V_{CC} - V_{RC} - V_{BE} = V_{CC} - I_{C2}R_C - V_{BE} \quad -(3)$$

$$V_0 = 10V - (1mA \times 6.8k\Omega) - 0.7V = 2.5V$$

⇒ Case 2: when a positive going i/p signal is applied at NON-INV i/p and INV i/p is grounded.

→ As V_{B1} increases due to V_i, so V_{E1} increases I_{E1} increases therefore I_{E2} decreases and hence I_{C2} decreases.

$$\because (\downarrow) I_{E2} = \frac{V_{RE}}{R_E} - I_{E1}(\uparrow)$$

Hence o/p voltage increases

$$(\uparrow) V_0 = V_{CC} - (\downarrow) I_{C2} R_C - V_{BE}$$

From eq (3) $V_0 = 10V - (0.8mA \times 6.8k\Omega) - 0.7V = 3.9V$

(I_{C2} is reduced to 0.8mA, 1mA − 0.2mA)

⇒ Case 3:- when a +ve going i/p at Non-INV produces positive going output vtg.

→ As $V_{B2}\uparrow$, V_{E2} also increases

$$\because (\uparrow) V_E = (\uparrow) V_B - V_{BE}$$

So I_{E2} increases $\left[I_E = \frac{V_E}{R_E}\right]$ and also I_{C2} increases

$$\because I_C = \beta I_B, \quad I_C = I_E$$

Hence o/p vtg decreases

$$\because \downarrow V_0 = V_{CC} - (\uparrow) I_{C2} R_C - V_{BE}$$

From eq(3) $V_0 = 10V - (1.2mA \times 6.8k\Omega) - 0.7V = 1.1V$

(I_{C2} is increased to 1.2mA, 1mA + 0.2mA)

→ In case 2, a positive going i/p at Non-INV terminal produces positive going o/p vtg

→ In case 3, a positive going i/p at INV terminal produces a negative going o/p vtg

2. Explain the working of a basic operational amplifier ckt with $R_C = 7.5k\Omega$, $R_E = 3.8k\Omega$ & powered by ±12V supply.

Refering to Figure 1.

→ Working can be explained by considering 3 cases.

⇒ Case 1: when two i/p terminals are grounded.

Let Q_1 and Q_2 are matched transistors i.e $V_{BE1} = V_{BE2}$ & $\beta_1 = \beta_2$ ∴ $I_{E1} = I_{E2}$ flows through common R_E

$\therefore I_E = I_{E1} + I_{E2} = \frac{V_{RE}}{R_E}$ -(1)

$V_{RE} = -V_{BE} - V_{EE} = -0.7 - (-12)$

$= 11.3V$

but $\because I_E = \frac{11.3V}{3.8k\Omega} = \frac{V_{RE}}{R_E} = 2.97mA.$

Since $I_{E1} = I_{E2} \Rightarrow I_{C1} = I_{C2} = I_{E1} + I_{E2}$

$= \frac{I_E}{2} = \frac{2.97mA}{2} = 1.48mA$

$V_{RC} = I_{C2} \times R_C = 1.48mA \times 7.5k\Omega = 11.14V$

From eq (3) $V_0 = V_{CC} - I_{C2}R_C - V_{BE}$

$= 12 - 11.14 - 0.7 = 0.16V.$

⇒ <u>Case 2</u>: when a +ve going i/p signal is applied at Non-INV i/p & INV i/p is grounded.

→ As V_{B1} increases due to V_i, V_{E1} increases. So I_{E1} increases & Therefore I_{E2} decreases and hence I_{C2} decreases

$\because (\downarrow) I_{E2} = \frac{V_{RE}}{R_E} - I_{E1}(\uparrow)$

Hence o/p vtg increases

$(\uparrow) V_0 = V_{CC} - (\downarrow) I_{C2}R_C - V_{BE}$

→ A +ve going i/p at NON-INV terminal produces +ve going o/p vtg.

⇒ <u>Case 3</u>: when a +ve going i/p signal applied at INV i/p and Non-INV i/p is grounded.

→ As V_{B2} increases due to V_i, V_{E2} also increases.

$\because \uparrow V_E = (\uparrow) V_B - V_{BE}$.

So I_{E2} increases and also I_{C2} ($\because I_C = I_E$)

Hence o/p vtg decreases

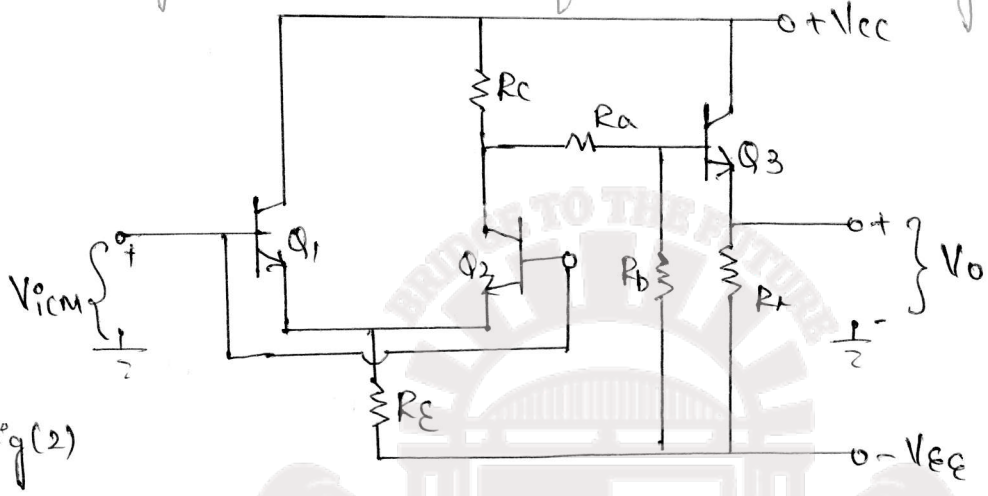
$\because (\downarrow) V_0 = V_{CC} - (\uparrow) I_{C2}R_C - V_{BE}$

→ A positive going i/p at inverting input terminal produces a negative going output voltage.

3. → Explain common mode voltage, common mode voltage gain & Common mode Rejection Ratio for operational amplifier. show that $V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \times A$.

(OR)

→ Derive an expression to relate the input & output common mode voltage (V_{icm} & V_{ocm}) of a Non-inverting amplifier.



Fig(2)

⇒ Common mode voltage: In the above basic op-amp ckt if two terminals are shorted together and applied an i/p vtg V_{icm} between the shorted terminals and grounded. Those applied vtg is called "Common mode i/p vtg". For common mode i/p ideally o/p should be zero because differential voltage in zero.

⇒ Common mode vtg gain (A_{cm}): As V_{B1} & V_{B2} are raised by V_{icm}, then vtg drop across R_E will also increased by the same. which result in increased values of collector current I_{C1} & I_{C2}.

→ Common mode voltg gain gain A_{cm} is the output vtg change due to common mode i/p divided by the common mode i/p voltage.

$$A_{cm} = \frac{V_{o(cm)}}{V_{i(cm)}}$$

→ If Q_1 & Q_2 are raised to 1V above ground, the voltage drop across emitter resistor R_E is increased by 1V and I_{C1} & I_{C2} are increased.

→ The increased level of I_{C2} produces an increased vtg drop across resistor Rc, which result in a change in output voltge at emitter of Q_3.

⇒ Common mode Rejection Ratio: The CMRR is defined as the ability of an op-Amp to reject the common mode inputs or It is defined as the ratio of open loop gain M or to the common mode gain Acm.

$$CMRR = \frac{M}{A_{cm}} \quad -(1)$$

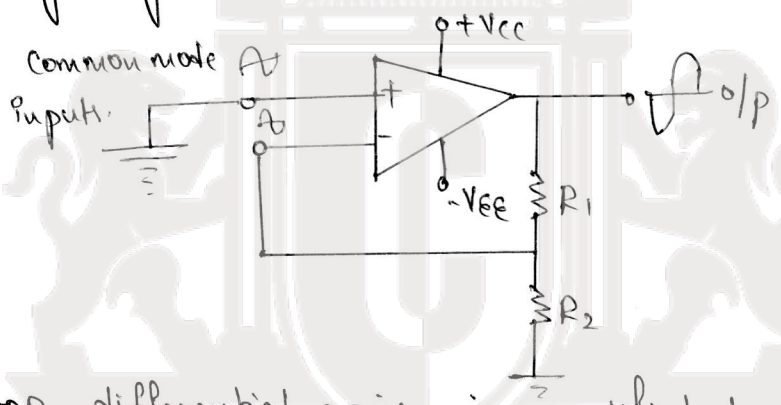
Usally CMRR is expressed in dB's

$$\therefore CMRR = 20 \log \left[\frac{M}{A_{cm}}\right] dB. \quad -(2)$$

and the typical value of CMRR is 90dB.

→ fig 3, It is amplified by the common mode gain, but the gain is affected by negative feedback.

fig 3



→ The open-loop differential gain is modified by feedback to give a closed loop gain and its gain is given by

$$A_{V(cm)} = \frac{V_{o(cm)}}{V_{i(cm)}}$$

$$\Rightarrow V_{o(cm)} = A_{cm} \times V_{i(cm)}$$

→ Any o/p vtg will produce a feedback voltage across resistor R_2, which results in differential vtg at the op-amp i/p terminals.

→ The differential i/p produces an o/p which tends to cancel the o/p vtg that caused the feedback.

→ The differential i/p vtg required to cancel $V_{o(cm)}$ is

$$V_d = \frac{V_{o(cm)}}{M} = \frac{A_{cm} \times V_{i(cm)}}{M}$$

→ V_d is the feedback vtg developed across R_2.

$$V_d = \frac{V_{o(cm)} \times R_2}{R_1 + R_2}$$

$$\frac{V_{o(cm)} \times R_2}{R_1 + R_2} = \frac{A_{cm} \times V_{i(cm)}}{M}$$

$$V_{o(cm)} = \frac{A_{cm} V_{i(cm)}}{M} \times \frac{R_1 + R_2}{R_2}$$

$$V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \times A_V \qquad \left[CMRR = \frac{M}{A_{cm}}\right]$$

4. Define CMRR of an op-amp. If a Non inverting amplifier is designed for a gain of 100, using an op-amp with 95dB CMRR. Calculate the common mode output (V_{ocm}) for a common mode i/p (V_{icm}) of 2V.

Referring to fig 2.

$A_V = 100$, $V_{icm} = 2V$, $CMRR = 95dB$

$V_{oCm} = ?$

From eq (2) $\quad CMRR = \text{antilog} \frac{95dB}{20} = 56234$

$$V_{ocm} = \frac{V_{icm}}{CMRR} \times A_V = \frac{2}{56234} \times 100$$

$$V_{ocm} = 3.55 \times 10^{-3} = 3.55 mV.$$

5. give definitions of the following op-amp parameters & give their typical values for 741 op-amp.

(i) CMRR (ii) PSRR

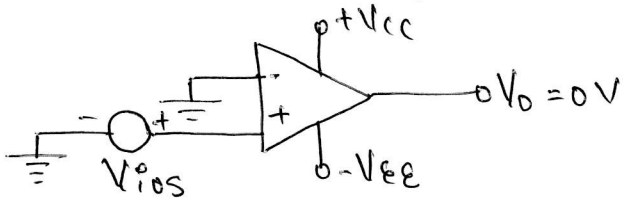
(iii) Input offset voltage (iv) Slew Rate.

(i) <u>CMRR</u>: The success of the op-amp in rejecting common mode inputs is defined as common mode Rejection Ratio.

$$CMRR = \frac{M}{A_{cm}} = \frac{\text{open loop gain}}{\text{common mode voltage gain}}$$

typical value of common mode Rejection Ratio = 90dB.

(ii) Input offset voltage: The input vtg used to nulling the output voltage is termed as i/p offset voltage



→ V_{ios} is the extra voltage applied to make the o/p vtg zero with zero input.

→ With zero input, we expect the o/p vtg to be zero but practically due to unmatched transistors (i.e $V_{BE1} \neq V_{BE2}$) o/p vtg may not be zero all the times.

i.e. $V_0 = V_i - V_{BE1} + V_{BE2}$

if $V_{BE1} = V_{BE2}$ $V_0 = V_i$ ⇒ $V_i = 0$ then $V_0 = 0$

if $V_{BE1} \neq V_{BE2}$ & $V_i = 0$

then $V_0 = 0 + V_{BE2} - V_{BE1}$

$= 0.7 - 0.6 = 0.1V$

where 0.1V is the o/p offset voltage.

→ The typical value of input offset vtg for 741 op-amp is 1mV.

⇒ (iii) PSRR (power supply Rejection Ratio):

→ It is defined as the ability of an op-amp in rejecting the power supply variations (or) It is a measure of how effectively the op-amp is in dealing with variations in power supply

$$PSRR = \frac{V_{o(ripple)}}{V_{s(ripple)}} \text{ or } \frac{\Delta V_o}{\Delta V_{CC} \text{ or } \Delta V_{EE}}$$

→ The typical value of PSRR for 741 op-amp is 30μV/V

[1V variation in Vcc or VEE causes the output voltage variation by 30μV]

⇒ (iv) Slew Rate: It is the maximum rate at which the output voltage can change, $t = \frac{\Delta V_o}{S}$.

The typical slew rate of 741 op-amp is 0.5V/μsec.

6. Define Slew Rate & Unit gain band width. What is the effect of slew rate on the output voltage of an op-amp?

⇒ Slew Rate (S): The slew rate of op-amp is the maximum rate at which the output voltage can change. The typical slew rate of 741 op-amp is 0.5V/μs means 1μs is time required for the output to change by 0.5V. The equation relating time, voltage change and slew rate is given as

$$t = \frac{\Delta V_o}{S}$$

→ Ideal value of slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to i/p step voltage. For large signal output, the op-amp's speed is limited by slew Rate.

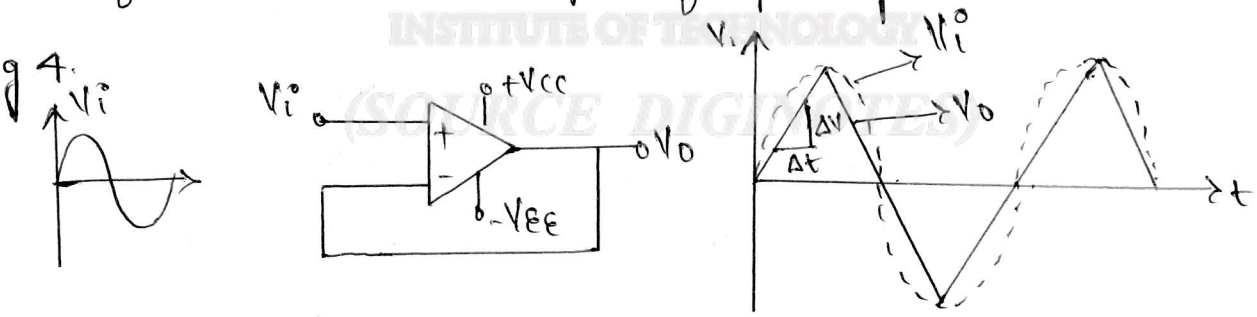
→ Slew rate is usally caused by a capacitor within or form responding immediately to a fast hanging o/p.

⇒ Unit gain Band width: It is the closed loop gain A_V multiplied by the cut-off frequency for that gain. For the unit gain frequency to closed loop gain A_V and the cut-off frequency f_2 is given as

$$A_V \cdot f_2 = f_u \quad (\text{or}) \quad f_2 = \frac{A_V}{f_u}$$

⇒ Effect of slew Rate on output of op-amp

Fig 4.

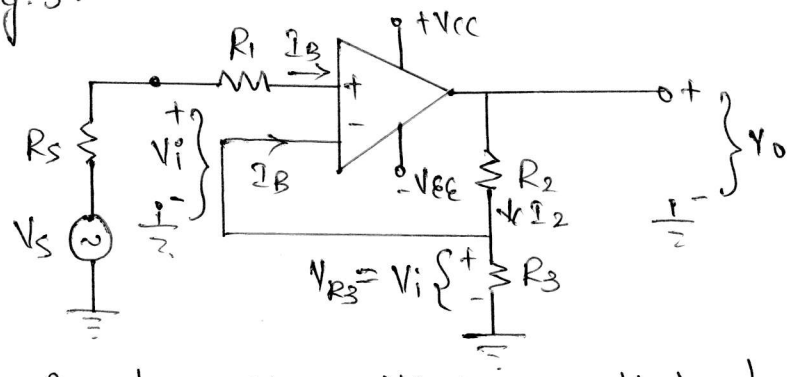


→ Let us consider, a vtg follower, applied with sine wave i/p, when the i/p vtg changes too fast, the o/p waveform distortion results.

→ When 'S' is too slow for i/p results in distortion. This is shown above a sinusoidal i/p produces a triangular o/p in a vtg follower ckt.

7. With a neat ckt diagram, explain direct coupled non-inv amplifier with necessary design steps.

Fig. 5.



→ The input voltage V_i is applied to non-inverting terminal of op-Amp, same voltage will appear at inverting terminal also.

→ open loop gain is infinity

$$A_{OL} = \infty = \frac{V_o}{V_d}$$

$$\Rightarrow V_d = \frac{V_o}{\infty} = 0$$

i.e $V_+ = V_-$

→ Vtg at inv and non-inv terminals are equal.

So $V_{R3} = V_i = I_2 R_3$

→ But o/p vtg is $V_o = I_2(R_2 + R_3)$

$I_B \sim 0$, because no current enters into the terminals of op-amp.

$$\text{Voltage gain} = A_V = \frac{V_o}{V_i} = \frac{I_2(R_2+R_3)}{I_2 R_3}$$

$$A_V = 1 + \frac{R_2}{R_3}$$

→ Difference amplifier, the difference between the two input signals V_1 and V_2.

⇒ <u>Design</u>:

→ For a bipolar op-amp, select the potential divider current (I_2) much larger than the maximum i/p bias current ($I_{B\,max}$)

i.e $I_B >> I_{B\,max} \Rightarrow I_2 = 100 I_{B\,max}$

→ For biFET op-amp, select the larger value resistor as 1MΩ.

$$R_3 = \frac{V_i}{I_2} \quad \& \quad V_o = A_V V_i$$

$$(R_2+R_3) = \frac{V_0}{I_2} \Rightarrow R_2 = \frac{V_0}{I_2} - R_3$$

→ To equalize the vtg drops at '+' & '−' terminals

$$R_1 = R_2 \| R_3$$

~~ext~~ exact value of R_1

$$R_1 + R_S = R_2 \| R_3 \quad \text{or} \quad R_1 = (R_2 \| R_3) - R_S.$$

8. A non-inverting amplifier is to amplify a 100mV signal to a level of 3V, using 741 op-amp design a suitable ckt.
[consider $I_{Bmax} = 500nA$, $R_S = 1k\Omega$]

$$I_2 = 100 I_{Bmax} = 100 \times 500 \times 10^{-9} A = 50\mu A$$

$$V_{R3} = V_i^o = I_2 R_3$$

Fig 6:

$$R_3 = \frac{V_1}{I_2} = \frac{100mV}{50\mu A} = 2k\Omega$$

use $1.8k\Omega$ standard value

Recalculate the value of I_2

$$\therefore I_2' = \frac{V_1}{R_3} = \frac{100mV}{1.8k\Omega} = 55.6\mu A$$

$$R_2 = \frac{V_0 - V_i^o}{I_2} = \frac{3-0.1}{55.6\mu A} = \frac{2.9V}{55.6\mu A} = 52.16k\Omega$$

using $47k\Omega + 5.6k\Omega$ in series

$$R_i^o = R_2 \| R_3 = 52.6k\Omega \| 1.8k\Omega = 1.8k\Omega.$$

$$R_1 = (R_2 \| R_3) - R_S = 1.8k\Omega - 1k\Omega = 0.8k = 800\Omega$$
(OR)

$$R_3 = 2k\Omega$$

$$I_2' = \frac{V_1}{R_3} = \frac{100mV}{2k\Omega} = 50\mu A$$

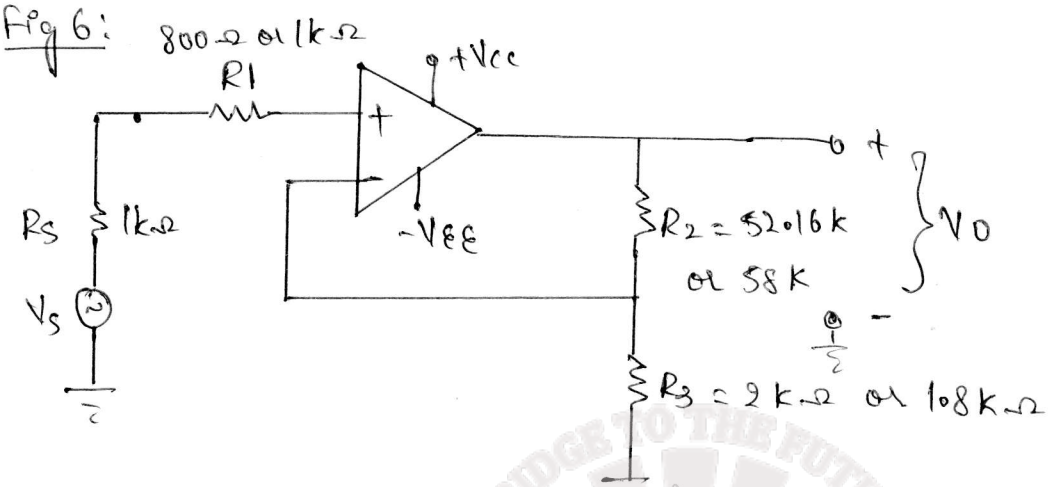
$$R_2 = \frac{V_0 - V_i^o}{I_2} = \frac{3-0.1}{50\mu A} = 58k\Omega$$

$$R_i^o = 2k\Omega \| 58k\Omega = 2k\Omega.$$

Considering R_s

$$R_1 = 2k\Omega - 1k\Omega$$
$$= 1k\Omega$$

Fig 6:



9. Design an inverting amplifier using op-amp 741. The vtg gain is to be 50. The o/p vtg amplitude is to be 2.5V.

$A_V = 50$, $V_o = 2.5V$

$$A_V = \frac{V_o}{V_i} \Rightarrow V_i = \frac{A_V \times V_o}{V_o} = \frac{2.5}{50} = 50mV$$

$$I_1 = 100 I_{Bmax} \qquad \because I_{Bmax} = 500nA$$
$$= 100 \times 500 \times 10^{-9} A$$
$$= 50\mu A$$

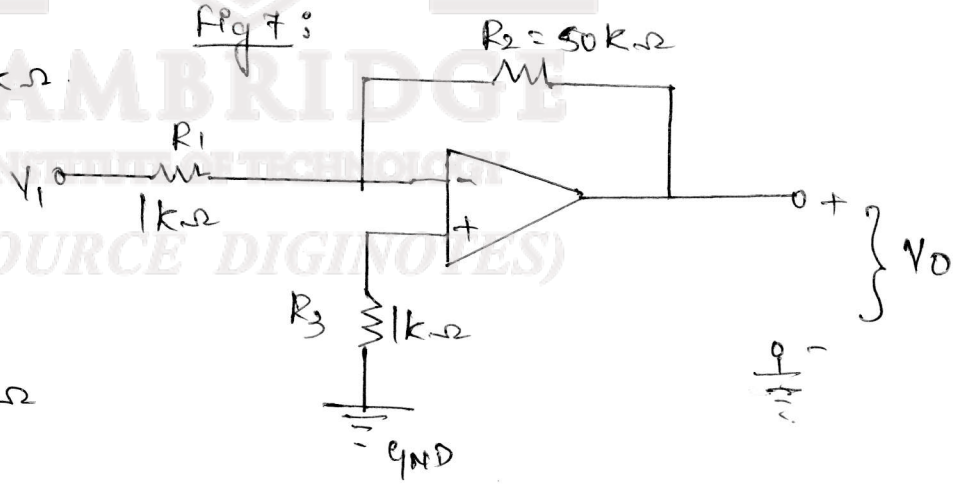
$$R_1 = \frac{V_1}{I_1} = \frac{50mV}{50\mu A} = 1k\Omega$$

$$A_V = -\frac{R_2}{R_1}$$

$$R_2 = A_V \times R_1$$
$$= 50 \times 1k\Omega = 50k\Omega$$

$$R_3 = R_1 \| R_2$$
$$= 1k\Omega \| 50k\Omega$$
$$= 1k\Omega$$

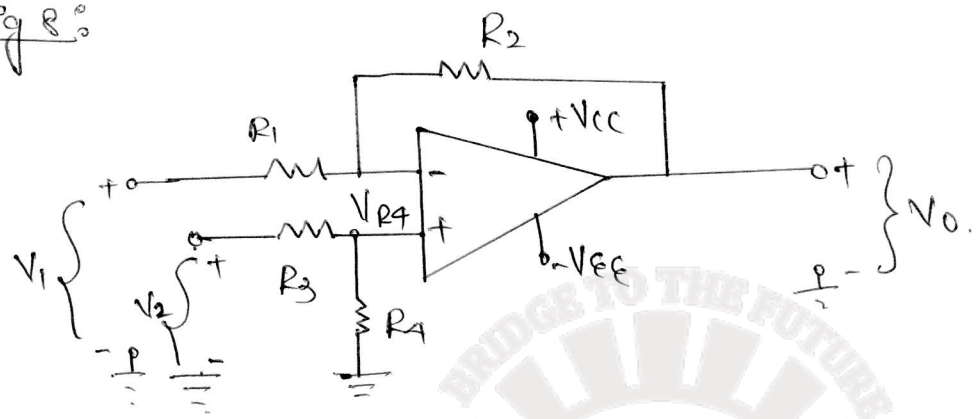
Fig 7:



10. Sketch an op-amp difference amplifier ckt. Derive an ~~expre~~ equation for the output voltage and explain the operation.

→ Difference amplifier amplifier the the difference between the two i/p signal V_1 and V_2.

Fig 8:



Using superposition theorem.

(i) with $V_2=0$, op-amp acts as inverting amplifier

$$\therefore V_{01} = -\frac{R_2}{R_1} V_1$$

(ii) with $V_1=0$, op-amp acts as non-inverting amplifier

The i/p vtg across R_4 is given as

$$V_{R4} = \frac{R_4}{R_3+R_4} \cdot V_2$$

o/p vtg is given as

$$V_{02} = V_{R4} \times \left[1 + \frac{R_2}{R_1}\right] \quad \text{or} \left\{ AV = \frac{\text{o/p vtg}}{\text{i/p vtg}} = \frac{V_{02}}{V_{R4}} \right\}$$

$$= \left[\frac{R_4}{R_3+R_4}\right]\left[\frac{R_1+R_2}{R_1}\right] V_2$$

when $R_3 = R_1$ & $R_4 = R_2$

$$V_{02} = \frac{R_2}{R_1} \cdot V_2$$

Using Superposition principle

$$V_0 = V_{01} + V_{02} = -\frac{R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2$$

$$= \frac{R_2}{R_1}\left[V_2 - V_1\right]$$

when $R_2 = R_1$, $V_0 = V_2 - V_1$

when $R_2 > R_1$ $V_0 = \frac{R_2}{R_1}(V_2 - V_1)$

The o/p can be an amplified version of the i/p differences.

11. Two signals each ranging from 0.1V to 1V are to be summed using 741 op-amp design a suitable inverting summing ckt.

$I_1 = 100 I_{Bmax}$

$= 100 \times 500nA$

$= 50\mu A$

$R_1 = \frac{V_{S\,min}}{I_{1\,min}} = \frac{0.1}{50\mu A} = 2K\Omega$

$R_1 = 1.8K\Omega$ (standard value)

$\therefore A_V = 1$, $R_3 = R_1 = 1.8K\Omega$

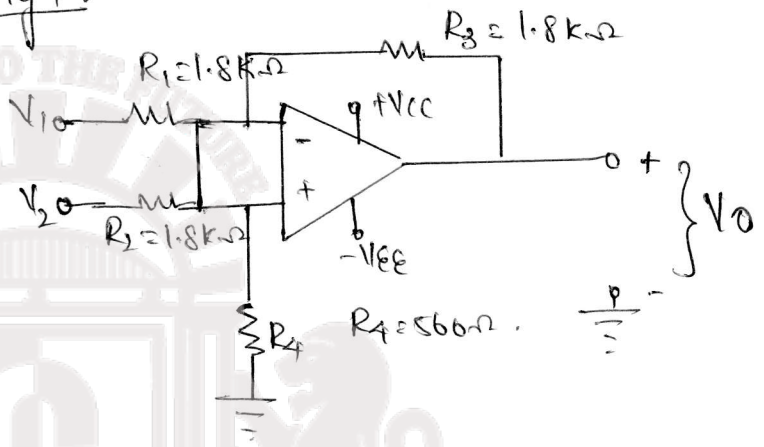
$R_4 = R_1 \| R_2 \| R_3$

$= 1.8k \| 1.8k \| 1.8k$

$= 600\Omega$

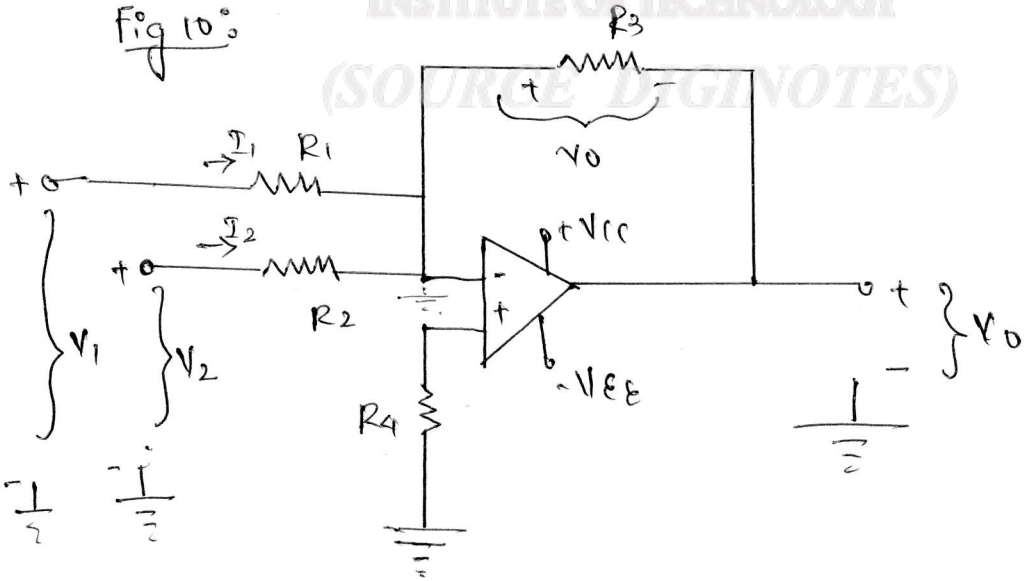
$= 560\Omega$ (standard value)

Fig 9:



12. Sketch the ckt of a two-i/p inverting summing amplifier. Explain the operation of the ckt and derive the equation for the o/p v/tg

Fig 10:



Inverting summing amplifier amplies the sum of two or more inputs.

→ Due to virtual ground effect, current flowing through R_1 & R_2 is given as

$$I_1 = \frac{V_1}{R_1} \quad \& \quad I_2 = \frac{V_2}{R_2}$$

→ All of $(I_1 + I_2)$ flows through resistor R_3.

$$-(I_1 + I_2) R_3 + V_0 = 0$$

$$\Rightarrow V_0 = -(I_1 + I_2) R_3$$

$$V_0 = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] R_3$$

→ when $R_1 = R_2$

$$V_0 = -\frac{R_3}{R_1}[V_1 + V_2]$$

where closed loop gain $= -\frac{R_3}{R_1}$

→ when $R_1 = R_2 = R_3$

$$V_0 = -1[V_1 + V_2]$$

→ the output is direct sum of the i/p voltage inverted with $R_3 > R_1 + R_2$.

→ The sum is applied by $\frac{R_3}{R_1}$ times

⇒ <u>Design:</u>

$$R_1 = \frac{V_S}{I_1} = \frac{V_S}{100 I_{Bmax}}$$

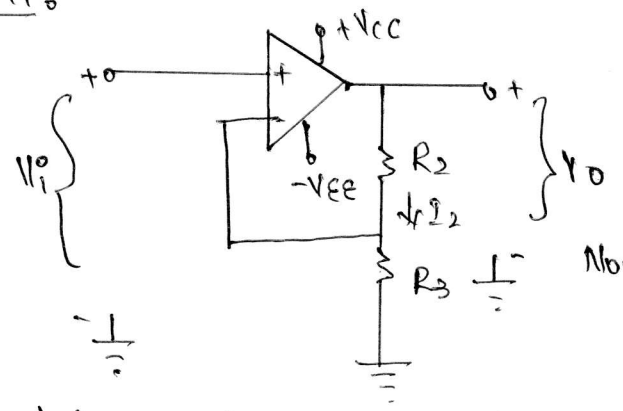
$$R_1 = R_2$$

Depending on gain, A_{CL} select R_3 as $R_3 = A_V R_1$

R_4 compensating resistor $R_4 = R_1 \| R_2 \| R_3$.

13. Sketch the complete ckt of an op-amp non-inverting amplifier. Write equations for determining suitable values for each resistances (i) using a bipolar op-amp & (ii) using a bifet op-amp.

Fig 11:



Non-Inverting amplifier.

→ It behaves in similar to voltage follower circuit. The difference is instead of all of the o/p being fed directly back to i/p, only a portion is fed back.

→ The o/p vtg is potentially divided across resistors R_2 and R_3 before it is applied to the inverting i/p.

→ When inv terminal is grounded, like vtg follower vtg drop across is also at ground level, otherwise any vtg difference would be amplified to move the inv i/p terminal back to ground level.

→ Their is vtg drop across R_3 because V_{R3} equal to zero & current through (I_2) R_2 & R_3 is also zero.

$$V_{R2} = V_i = I_2 R_3$$

$$V_0 = I_2 (R_2 + R_3)$$

$$AV = \frac{V_0}{V_1} = \frac{I_2 (R_2 + R_3)}{I_2 R_3}$$

$$AV = \frac{R_2 + R_3}{R_3}$$

14. Design a Non-Inv amplifier to provide a gain of 50 for an i/p of 100mV. Compute its i/p & o/p impedances. gn $R_i = 2M\Omega$, $R_o = 75\Omega$, $I_{Bmax} = 500nA$, & $M = 2,00,000$. for the op-amp 741.

i/p impedence $Z_{in} = [1+m\beta] Z_i$

o/p impedence $Z_{out} = \dfrac{Z_o}{1+m\beta}$

$\beta = \dfrac{1}{A_V}$ for non-inv amplifier.

$$Z_{in} = \left[1 + \frac{2\times10^5}{50}\right] Z_i$$

$$\boxed{Z_{in} = 8.002 \times 10^9 \Omega}$$

$$Z_{out} = \frac{Z_o}{1+m\beta}$$

$$Z_{out} = \frac{75\Omega}{1 + 2,00,000\left(\frac{1}{50}\right)}$$

$$\boxed{Z_{out} = 0.0187\Omega}$$

16. Design a bias current compensated inverting amplifier to amplify a dc i/p of 150mV by a β factor of 40. Use a bipolar op-amp with $I_{Bmax} = 500nA$.

$V_i = 150mV \quad A_V = 40$

$A_V = \frac{V_o}{V_i} \Rightarrow V_o = A_V V_i = 40 \times 150mV = 6V$

$I_1 = 100 I_{Bmax} = 50\mu A$

$R_1 = \frac{V_1}{I_1} = \frac{150mV}{50\mu A} = 3k\Omega$

$= 2.7k\Omega$ a standard value

$A_V = \frac{R_2}{R_1}$

$R_2 = A_V \times R_1$

$= 40 \times 3k\Omega$

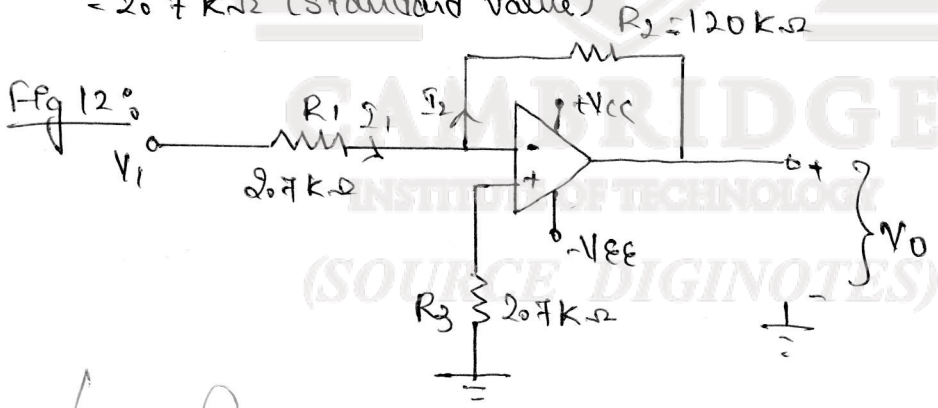
$= 120k\Omega$

$R_3 = R_1 \| R_2 = 3k\Omega \| 20k\Omega$

$= 2.93k\Omega$

$= 2.7k\Omega$ (standard value)

Fig 12:



(Lateefa A.M)

Name & Signature of the Course Instructor

Design a differential amplifier for a gain of 100. If the i/p vtg $V_1 = 10V$ & $V_2 = 10.01$ to $10.1V$. Calculate impedences at V_1, V_2. Common mode & differential. use 741 op-amp.

Soln.

Given $A_v = 100$

$V_1 = 10V$

$V_2 = 10.01$ to $10.1V$

$$R_i = \frac{V_i(min)}{I_i}$$

$I_i = 100\, I_{Bmax}$

$= 100 \times 500nA$.

$$R_1 = \frac{10}{50\mu A}$$

$R_1 = 200k\Omega$

$$A_v = \frac{R_2}{R_1}$$

$R_2 = A_v R_1$

$R_2 = 20M\Omega$.

Op-amp as ac Amplifiers

Introduction:-

→ op-amp can be used as dc as well as ac amplifiers

→ For op-amp ac amplifiers, the coupling capacitors are necessary at the input as well as output terminals. These capacitors must not be allowed to interrupt the bias current paths to the op-amp input terminals.

This sometimes require additional bias resistors which can affect the circuit i/p impedance

→ Since the capacitors have their highest impedances at the lowest signal frequency, all the coupling capacitor values are determined at the lower cut-off frequency 'f_1'

→ The impedance of coupling capacitors at f_1 is usually one-tenth of the resistance in series with them.

AC-coupled Voltage follower:-

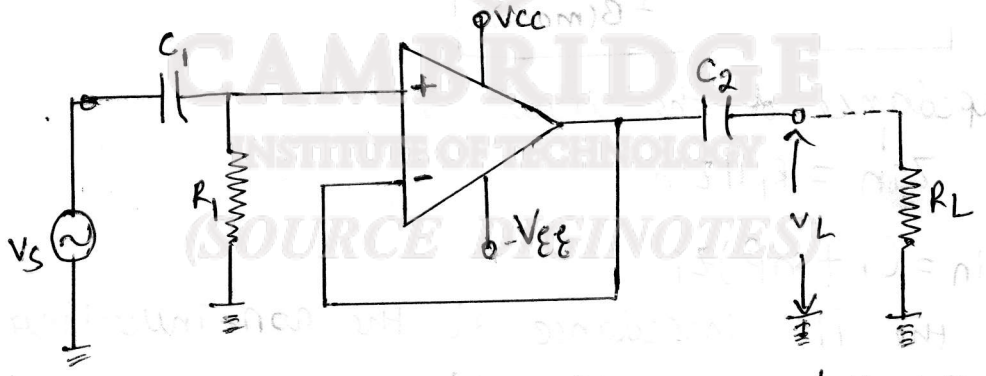


fig ① - Capacitor coupled voltage follower circuit

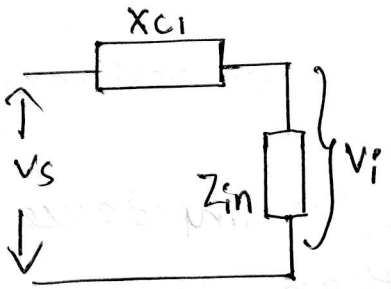


fig ② - The signal voltage is divided across X_{C_1} & Zin.

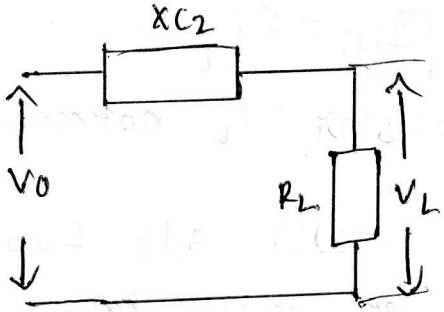


fig ③

The o/p voltage is divided across X_{C_2} & R_L

→ When a voltage follower is to have its i/p & o/p capacitor-coupled, the non-inverting terminal must be grounded via a resistor 'R_1'.

→ This resistor is required to pass the bias current to the amplifier non-inverting terminal

→ A resistor equal to 'R_1' might be included in series with the inverting terminal to equalize the $I_B R_B$ voltage drop & thus minimize the output offset voltage.

→ The o/p capacitor C_2 blocks the small dc offset voltage

Design:-

Design involves calculation of R_1, C_1 & C_2.

→ The smallest possible capacitor values are normally used for their small physical size & low cost.

→ The maximum value of R_1 is determined as.

$$\boxed{R_{1(max)} = \frac{0.1\, V_{BE}}{I_{B(max)}}}$$

→ I/p impedance of the circuit is.

$$Z'_{in} = R_1 \| Z_{in}.$$

where:-

$$Z_{in} = (1+m\beta) Z_i$$

Z_{in} is the i/p impedance at the non-inverting terminal & is very much larger than R_1

$$\therefore \boxed{Z'_{in} = R_1}$$

→ Load resistor R_L normally has a lower resistance than R_1.

→ At the lower 3db frequency 'f_1', the impedance of C_1 should be much smaller than Z_{in}.

$\therefore$ At f_1, $X_{C_1} = \frac{R_1}{10}$.

$$\frac{1}{2\pi f C_1} = \frac{R_1}{10}$$

$$\therefore \boxed{C_1 = \frac{1}{2\pi f\left(\frac{R_1}{10}\right)}}$$

From fig (3), the load voltage V_L is given by

$$V_L = I R_L$$

$$V_L = \frac{V_0 R_L}{R_L - j X_{C_2}}$$

$\therefore$ magnitude of $V_L = \frac{V_0 R_L}{\sqrt{R_L^2 + X_{C_2}^2}}$

when $X_{C_2} = R_L$, then.

$$V_L = \frac{V_0 R_L}{\sqrt{R_L^2 + R_L^2}} = \frac{V_0 R_L}{\sqrt{2 R_L^2}} = \frac{V_0}{\sqrt{2}}.$$

$$V_L = \frac{V_0}{\sqrt{2}}. \quad \boxed{V_L = 0.707\, V_0}$$

i.e the circuit low 3 db frequency f_1 occurs, when

$$X_{C_2} = R_L.$$

$\therefore X_{C_2} = R_L$ at f_1

$$\frac{1}{2\pi f C_2} = R_L.$$

$$\boxed{C_2 = \frac{1}{2\pi f R_L}}$$

High 'Zin' capacitor-coupled voltage follower:-

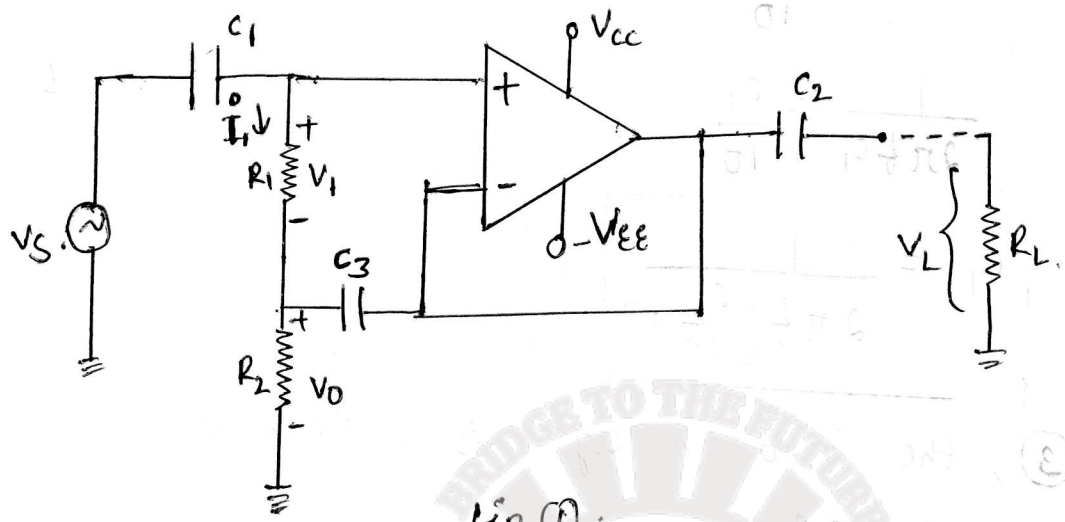


fig ①.

→ The i/p impedance of the capacitor-coupled voltage follower is set by the value of resistor R_1. This gives a much smaller input impedance than the direct coupled voltage follower.

→ fig ① shows a method by which the i/p impedance of the capacitor-coupled voltage follower can be substantially increased.

→ Capacitor C_2 couples the circuit o/p voltage to the function of resistors R_1 & R_2.

C_2 behaves as an ac short circuit. so that 'V_o' is developed across R_2.

→ Applying KVL from source, R_1 & R_2,

$$V_S - V_1 - V_o = 0$$

The voltage across R_1 is V_1 & is given by

$$V_1 = V_S - V_o \quad \rightarrow ①$$

W.K.T open-loop gain is given by $m = \frac{V_o}{V_i}$

$$V_o = mV_1 \rightarrow ②$$

substitute eqⁿ ② in eqⁿ ①, we get

$$V_1 = V_S - mV_1$$

$$mV_1 + V_1 = V_S.$$

$$V_1(1+m) = V_s.$$

$$\boxed{V_1 = \frac{V_s}{1+m}} \rightarrow (3)$$

→ The current i_1 is given by:

$$i_1 = \frac{V_1}{R_1} \rightarrow (4)$$

sub eq (3) in eq^n (4), we get

$$\boxed{i_1 = \frac{V_s}{(1+m)R_1}} \rightarrow (5)$$

→ I/p resistance

$$Z_{in} = \frac{V_s}{i_1} \rightarrow (6)$$

sub eq^n (5) in eq (6), we get

$$Z_{in} = \frac{\cancel{V_s}}{\frac{\cancel{V_s}}{(1+m)R_1}}$$

$$\boxed{Z_{in} = (1+m)R_1} \rightarrow (7)$$

∴ since open-loop gain 'm' is very high, this modifies the circuit has very high i/p impedance.

Capacitor Coupled Non-inverting amplifier:-

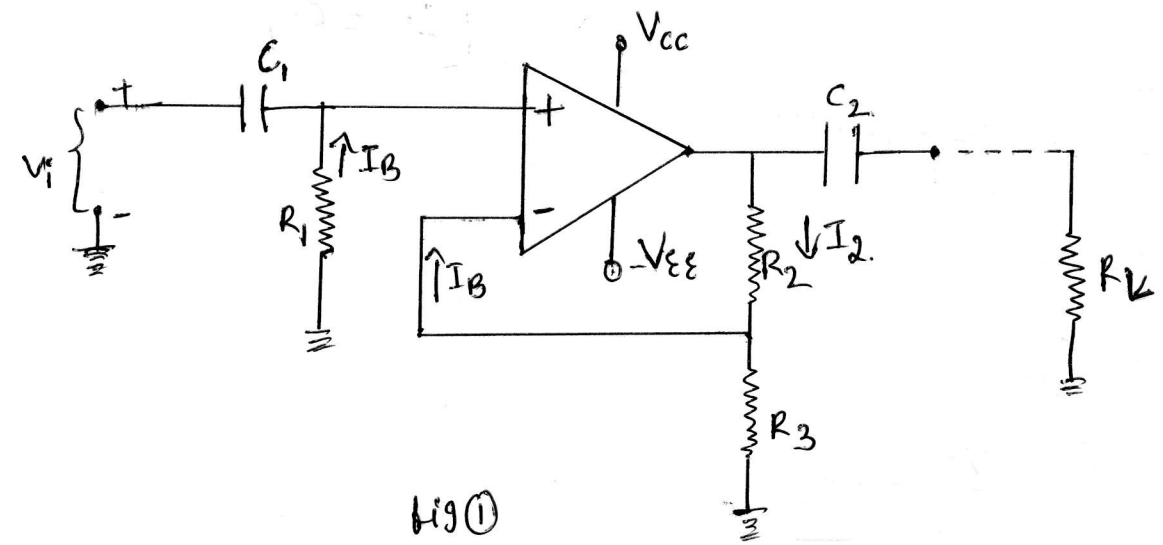


fig (1)

→ In capacitor-coupled non-inverting amplifier, the non-inverting i/p terminal is grounded via a resistor to provide a path for the i/p bias current.

→ The resistor R_1 may be made equal to $R_2 \| R_3$ to compensate for the dc offset voltage at the o/p.

Since the o/p is also capacitor coupled, it is not of much importance.

→ As in the case of the capacitor-coupled voltage follower, $Z_{in} = R_1$ for a capacitor coupled non-inverting amplifier.

→ Resistors R_2 & R_3 are calculated exactly as for a direct-coupled circuit & the capacitors are determined as for the capacitor-coupled voltage follower.

Design steps:-

* $R_1 = R_{1(max)} = \dfrac{0.1 V_{BE}}{I_{B(max)}}$

* $X_{C_1} = \dfrac{R_1}{10}$ at f_1, $C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$

* $X_{C_2} = R_L$ at f_1, $C_2 = \dfrac{1}{2\pi f_1 R_L}$

* $I_2 = 100 I_{B(max)}$

* $R_3 = \dfrac{V_i}{I_2}$.

* input impedance.

$\boxed{Z_{in} = R_1}$

* $A_V = \dfrac{V_o}{V_i}$ & $V_o = A_V V_i$

* $V_o = I_2 (R_2 + R_3)$

$\dfrac{V_o}{I_2} = R_2 + R_3$.

$R_2 = \dfrac{V_o}{I_2} - R_3$.

High "Z_{in}" Capacitor-Coupled Non-inverting Amplifier.

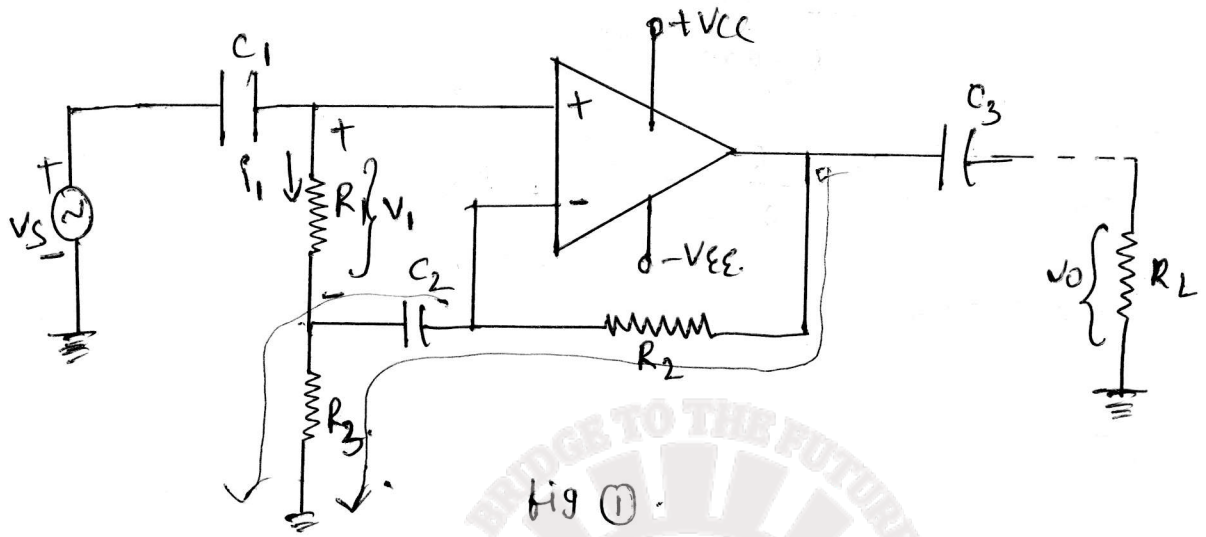


fig (1).

→ The input impedance of the non-inverting amplifier can be improved by using capacitor C_2. The voltage is fed back from the o/p to the i/p via R_2, C_2 & R_3.

→ The feedback factor 'β' is given by

$$A_V = \frac{1}{\beta} = \beta = \frac{1}{A_V} = \frac{1}{\frac{R_2+R_3}{R_3}}$$

$$\boxed{\beta = \frac{R_3}{R_2+R_3}}$$

→ The input impedance is given by

$$\boxed{Z_{in} = (1+m\beta)R_1}$$

Design steps :-

→ The resistance values of R_2 & R_3 for the high Z_{in} circuit are determined exactly as for a direct coupled non-inverting amplifier.

$$R_1 + R_3 = R_2.$$

which usually gives. $R_1 \approx R_2$

* $R_1 + R_3 = R_1(max)$

$$R_1 + R_3 = R_1(max) = \frac{0.1\, V_{be}}{I_{B(max)}}$$

* $A_V = 1 + \frac{R_2}{R_3}$ $\therefore$ $R_3 = \frac{R_2}{A_V - 1}$

* $R_1 = R_1(max) - R_3$.

* $A_V = \frac{V_o}{V_i}$

$$= \frac{I_2(R_2 + R_3 - jX_{C_2})}{I_2(R_3 - jX_{C_2})}$$

$$= \frac{R_2 + R_3 - jX_{C_2}}{R_3 - jX_{C_2}}$$

If $X_{C_2} << (R_2 + R_3)$

$$A_V = \frac{R_2 + R_3}{R_3 - jX_{C_2}}$$

Taking magnitude of denominator

$$= \frac{R_2 + R_3}{\sqrt{R_3^2 + X_{C_2}^2}}$$

Replace $X_{C_2} = R_3$

$$A_V = \frac{R_2 + R_3}{\sqrt{2 R_3^2}} = \left(\frac{R_2 + R_3}{R_3}\right)\left(\frac{1}{\sqrt{2}}\right)$$

* $X_{C_3} = \frac{R_L}{10}$ at f_1 $\Rightarrow$ $\boxed{C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)}}$

* $X_{C_2} = R_3$ at f_1 $\Rightarrow$ $\boxed{C_2 = \frac{1}{2\pi f_1 R_3}}$

Problems :-

1. Design Z_{in} capacitor coupled voltage follower using an op-amp having lower cut-off frequency of 50Hz & maximum input bias current of 500nA. The load resistance is 3.6kΩ. If the open loop gain is 2×10^5. Find ideal value of input impedance of the circuit.

Sol^n:- given :-

* $f_1 = 50Hz$ * $I_{B(max)} = 500nA$
* $R_L = 3.6k\Omega$ * $m = 2\times10^5$

* $R_1(max) = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1\times0.7}{500nA} = 140k\Omega$

* $X_{C_1} = \frac{R_1}{10}$ at f_1

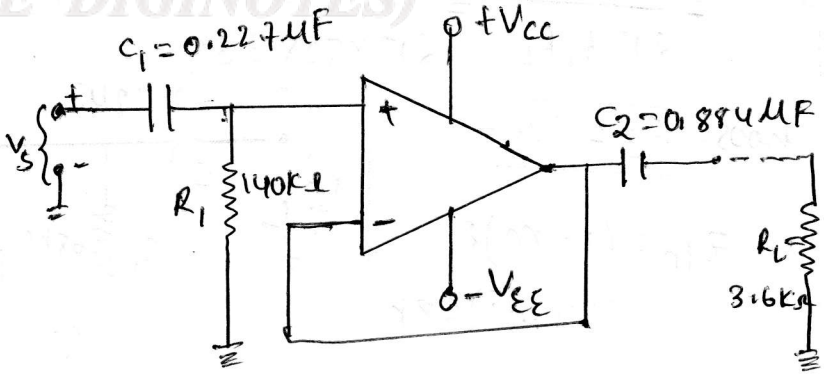
$$C_1 = \frac{1}{2\pi f_1\left(\frac{R_1}{10}\right)} = \frac{1}{2\pi(50)\left(\frac{140k}{10}\right)} = \boxed{C_1 = 0.227\mu F}$$

* $X_{C_2} = R_L$ at f_1

$$C_2 = \frac{1}{2\pi f_1 R_L}$$

$$= \frac{1}{2\pi(50)(3.6k)}$$

$$\boxed{C_2 = 0.884\mu F}$$



* $Z_{in} = (1+m)R_1$

$= (1+2\times10^5)140k$.

$Z_{in} = 2.8\times10^{10}\Omega$.

② Design high Z_{in} capacitor coupled voltage follower using an op-amp having lower cut-off frequency of 50Hz & maximum i/p bias current of 500nA. The load resistance is 3.3kΩ, if open loop gain of op-amp is 10^5, find Ideal value of i/p impedance of the ckt.

Sol^n:- given

* $f_1 = 50Hz$ * $m = 10^5$
* $I_{B(max)} = 500nA$ * $R_L = 3.3k\Omega$

* $R_1(max) = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7}{500 \times 10^{-9}} = 140k\Omega$.

* $R_1 = R_2 = \frac{R_1(max)}{2} = \frac{140k\Omega}{2} = 70k\Omega$.

Choose $\boxed{R_1 = R_2 = 68k\Omega}$

* $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi(50)\left(\frac{68k}{10}\right)} = 0.468\mu F$

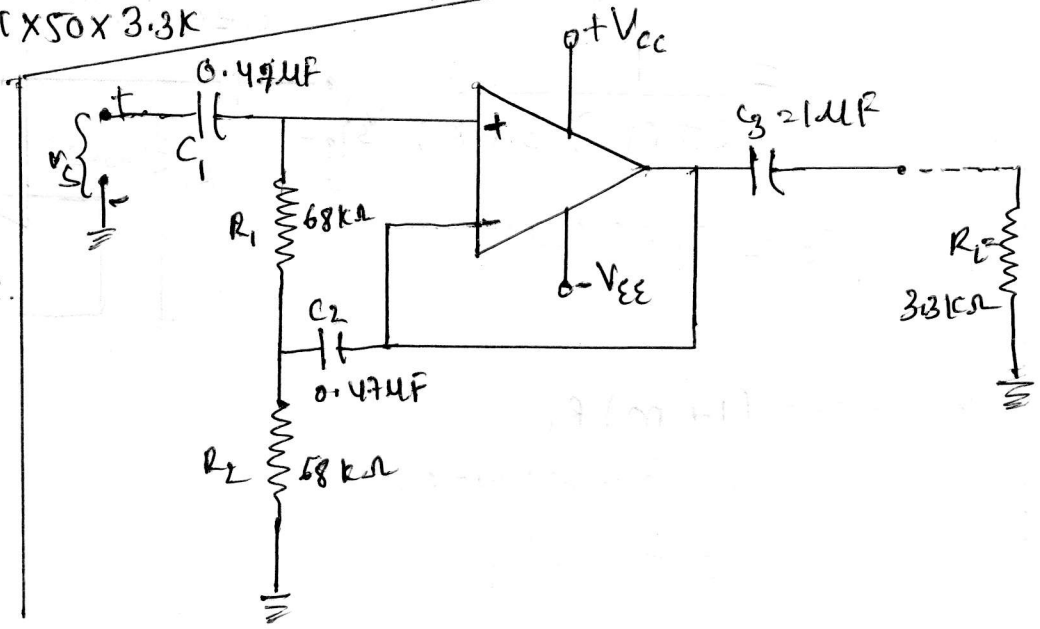
Choose $\boxed{C_2 = 0.47\mu F}$

* $C_1 = C_2 = 0.47\mu F$

* $C_3 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 3.3K} = 0.964\mu F$.

Choose $\boxed{C_3 = 1\mu F}$

* $Z_{in} = (1+m)R_1$
$= (1 \times 10^5)68K$.
$Z_{in} = 6800M\Omega$



Problems :-

1. A capacitor coupled non-inverting op-amp is to have $A_V = 100$, & $V_0 = 5V$ with $R_L = 10k\Omega$ & $f_1 = 100Hz$. Design suitable circuit.

Sol^n :- assume $V_{be} = 0.7V$.

1. $R_{1(max)} = \frac{0.1 V_{be}}{I_{B(max)}} = \frac{0.1 \times 0.7}{500n} = 140k\Omega$

2. $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi(100)\left(\frac{140K}{10}\right)}$ $\boxed{C_1 = 0.113\mu F}$

3. $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi(100)(10K)}$ $\boxed{C_2 = 0.159\mu F}$

4. $I_2 = 100\, I_{B(max)} = 50\mu A$

* $A_V = \frac{V_0}{V_i}$, $V_i = \frac{V_0}{A_V}$

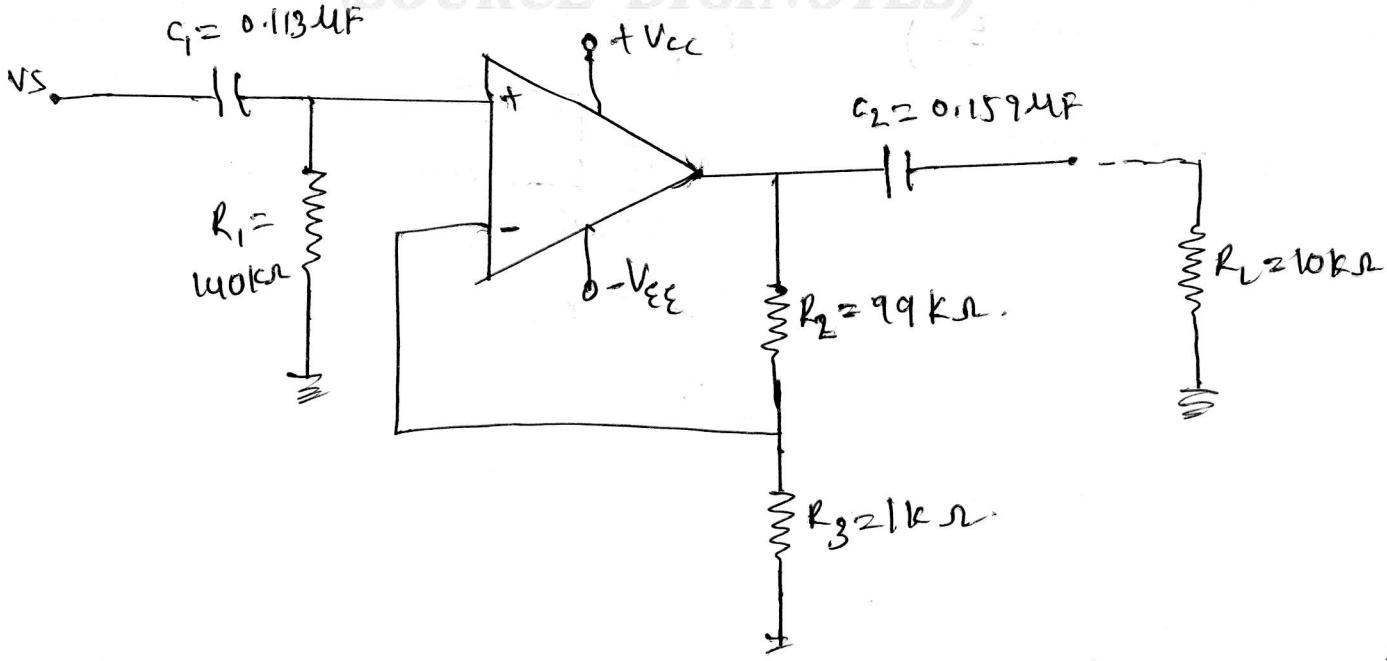
$V_i = \frac{5}{100} = 0.05V$ or $50mV$

5. $R_3 = \frac{V_i}{I_2} = \frac{50m}{50\mu}$

$\boxed{R_3 = 1k\Omega}$

6. $R_2 = \frac{V_0}{I_2} - R_3 = \frac{5}{50\mu} - 1k\Omega$

$\boxed{R_2 = 99k\Omega}$



(2) Using a LF 353 BIFET op-amp, design a high Zin capacitor coupled non-inverting amplifier to have a low cut-off frequency of 200 Hz. The i/p & o/p voltages are to be 15mV & 3 V respectively & minimum load resistance is 12 kΩ.

Given:-

$f_1 = 200\ Hz$, $V_o = 3V$, $V_i = 15mV$, $R_L = 12k\Omega$.

Sol^n:- $A_V = \frac{V_o}{V_i} = \frac{3}{15m}$ $\boxed{A_V = 200}$

* For LF 353 op-amp, select = $R_2 = 1m\Omega$.

* $R_3 = \frac{R_2}{A_V - 1} = \frac{1m}{200-1} = 5.025k\Omega$

* $R_1 = R_2 - R_3 = 1m - 5.025k = 995.7k\Omega$

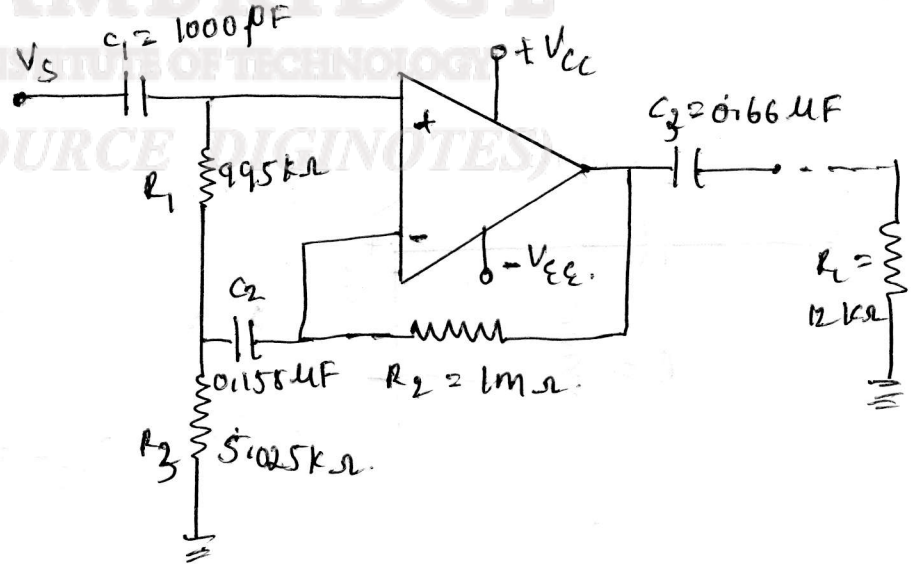
* $C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi(200)(5.025k)} = 0.158\mu F$

* choose $C_1 = 1000pF$

* $C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)}$

$= \frac{1}{2\pi(200)\left(\frac{12k}{10}\right)}$

$C_3 = 0.66\mu F$



Capacitor - Coupled Inverting Amplifier :-

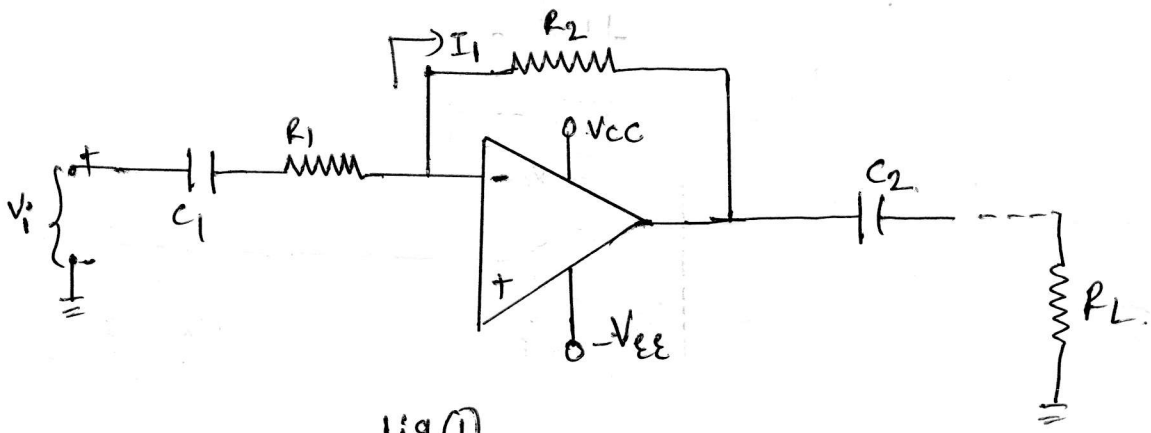


Fig ①

→ In capacitor coupled inverting amplifier, the bias current I_{B_1} to the op-amp inverting input terminal flows via resistor R_2. So the coupling capacitor C_1 does not interrupt the bias current.

→ No resistor is included in series with the non-inverting input terminal because of a small dc offset is unimportant with a capacitor coupled o/p.

→ The input impedance $\boxed{Z_{in} = R_1}$

Design steps :-

* $I_1 = 100 \times I_{B(max)}$

* $R_1 = \frac{V_i}{I_1}$

* $R_2 = \frac{V_o}{i_1}$

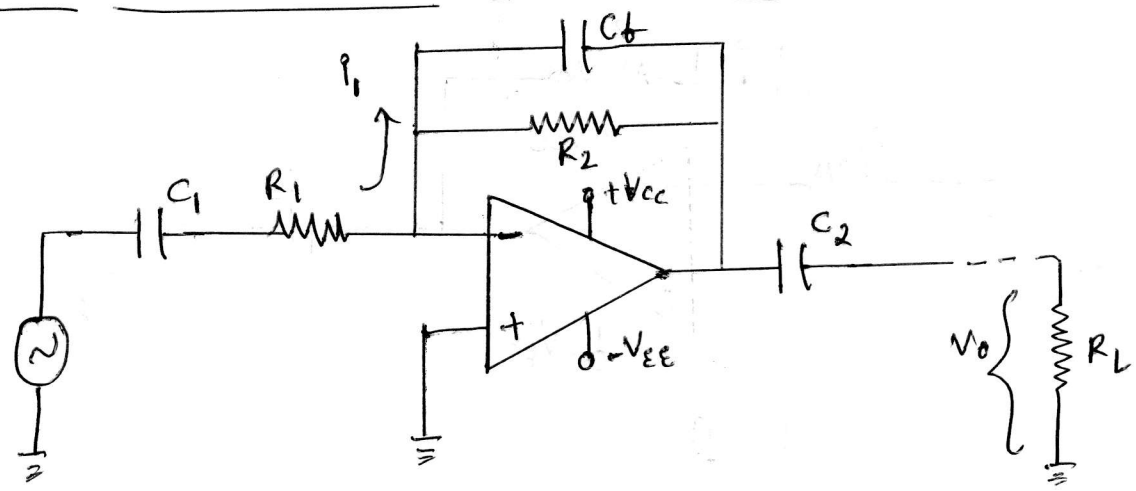
* $X_{C_1} = \frac{R_1}{10}$ at f_1

$$\boxed{C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}}$$

* $X_{C_2} = R_L$ at f_1 $\therefore$ $\boxed{C_2 = \frac{1}{2\pi f_1 R_L}}$

Setting the upper cut-off frequency:-

→



fig①

→ The highest signal frequency that can be processed by an op-amp circuit depends on the select op-amp.

For example: If very low frequency signals are to be amplified & unwanted higher frequency noise voltages are to be excluded.

→ If these high frequency noise voltages are to be eliminated, there must be a provision for their effective attenuation.

This can be achieved by setting the upper cut-off frequency just above the highest derived signal frequency.

This is done by connecting a feedback capacitor C_f from the op-amp o/p to its inverting i/p terminal as shown in fig①

* For inverting amplifier, the voltage gain is.

$A_V = \frac{R_2}{R_1}$. In fig① C_f is in parallel with R_2 so gain becomes

$$A_V = \frac{R_2 \| -jX_{Cf}}{R_1}$$

$$A_V = \frac{R_2(-jX_{Cf})}{R_1(R_2 - jX_{Cf})} = \frac{\cancel{R_2(-jX_{Cf})}}{\cancel{R_2(-jX_{Cf})}\left(\frac{1}{-jX_{Cf}} + \frac{1}{R_2}\right)}\left(\frac{1}{R_1}\right)$$

Taking the magnitude of denominator

$$A_V = \left(\frac{1}{\sqrt{\left(\frac{1}{R_2}\right)^2 + \left(\frac{1}{X_{Cf}}\right)^2}}\right)\left(\frac{1}{R_1}\right)$$

$$= \frac{1}{R_1}\left(\frac{1}{\sqrt{\left(\frac{1}{R_2}\right)^2 + \left(\frac{1}{X_{Cf}}\right)^2}}\right).$$

$X_{Cf} = R_2$ at f_2.

$$A_V = \frac{1}{R_1}\left(\frac{1}{\sqrt{\left(\frac{1}{R_2}\right)^2 + \left(\frac{1}{R_2}\right)^2}}\right)$$

$$= \frac{1}{R_1}\left(\frac{1}{\sqrt{\frac{2}{R_2^2}}}\right)$$

$$\boxed{A_V = \left(\frac{1}{\sqrt{2}}\right)\left(\frac{R_2}{R_1}\right)} \rightarrow (1).$$

The equation (1) indicates that the gain is 3db down the normal voltage gain.

→ Thus upper cut-off frequency f_2 for the circuit can be set to the desired frequency f_2 by making

* $\boxed{X_{Cf} = R_2}$ at f_2

$$\boxed{C_f = \frac{1}{2\pi f_2 R_2}}$$

* $X_{C_1} = \frac{R_1}{10}$ at f_2

$$\boxed{C_1 = \frac{1}{2\pi f_2\left(\frac{R_1}{10}\right)}}$$

* $X_{C_2} = \frac{R_L}{10}$ at f_2.

* $$\boxed{C_2 = \frac{1}{2\pi f_2\left(\frac{R_L}{10}\right)}}$$

Capacitor - Coupled differential amplifier:-

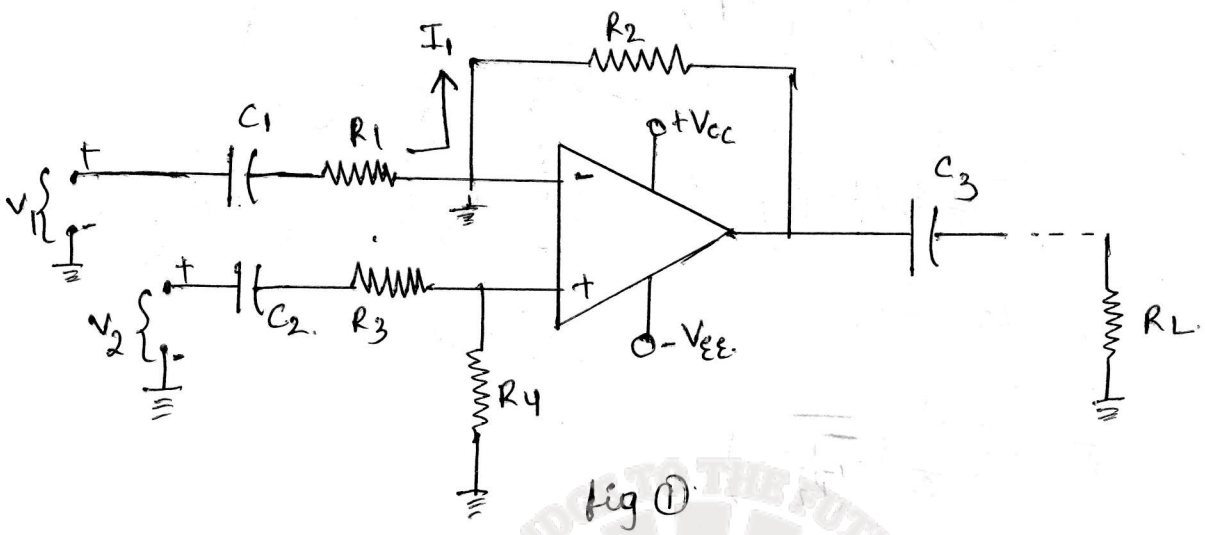


fig ①

→ fig ① shows a capacitor-coupled difference amplifier.

→ This circuit amplifies the difference between two signals applied at the non-inverting & inverting terminals of the op-amp.

→ Here again, the resistor values can be calculated in the same way as for a direct-coupled circuit & capacitors can be determined in the usual way.

→ The o/p voltage is given by

$$V_0 = V_2 - V_1$$

Design steps:-

* $I_1 = 100\, I_{B(max)}$
* $R_1 = \dfrac{V_1}{I_1}$
* $R_3 = R_1$
* $R_2 = \dfrac{V_0}{I_1}$
* $R_4 = R_2$
* $X_{C_1} = \dfrac{R_1}{10}$ at f_1, $\boxed{C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}}$
* $X_{C_2} = \dfrac{(R_3 + R_4)}{10}$ at f_1, $\boxed{C_2 = \dfrac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10}\right)}}$
* $X_{C_3} = R_L$ at f_1, $\boxed{C_3 = \dfrac{1}{2\pi f_1 R_L}}$

Problem :-

1. Design capacitor-coupled inv amplifier using op-amp 741 to have voltage gain of 100. assume signal voltage of 10mV & load of 4.7kΩ. choose $f_1 = 120$ Hz.

given :-

$A_V = 100$, $V_i = 10\,mV$, $R_L = 4.7\,k\Omega$, $I_{B(max)} = 500\,nA$

sol^n :-

* $I_1 = 100\, I_{B(max)} = 50\,\mu A$

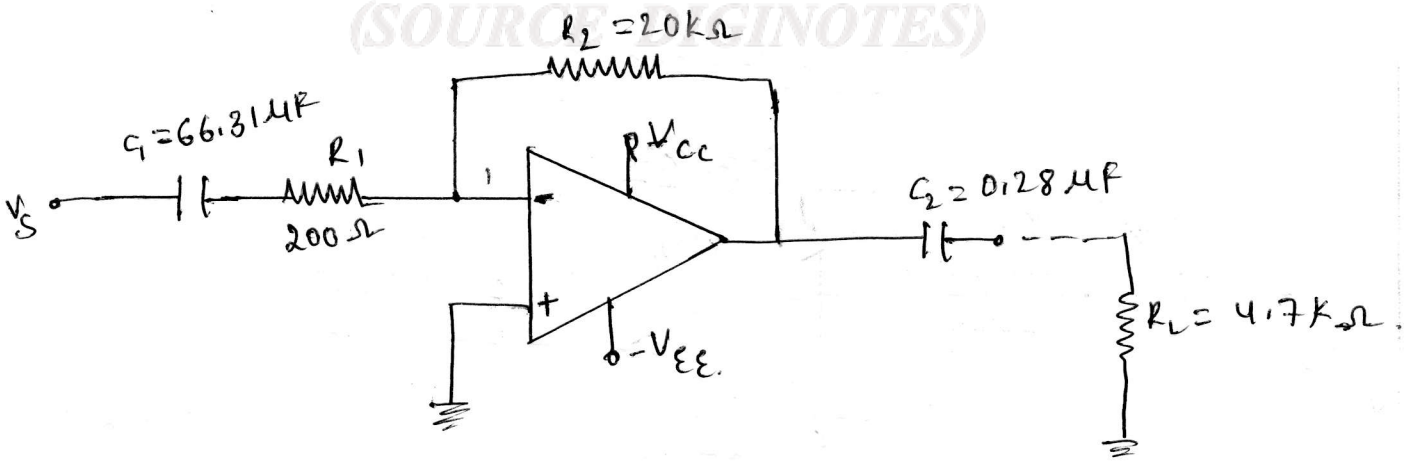
* $R_1 = \frac{V_i}{I_1} = \frac{10\,mV}{50\,\mu A} = 200\,\Omega$

w.k.T $A_V = \frac{R_2}{R_1}$

$R_2 = A_V R_1 = 100 \times 200 = \boxed{R_2 = 20\,k\Omega}$

* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi (120)\left(\frac{200}{10}\right)}$ $\boxed{C_1 = 66.31\,\mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi (120)(4.7k)}$ $\boxed{C_2 = 0.28\,\mu F}$



Setting upper cut-off frequency :-

Problem :-

① Design a c-coupled inverting amplifier for a pass-band gain of 100, $f_1 = 120\,Hz$ & $f_2 = 5\,kHz$. Assume $R_L = 2\,k\Omega$ & use the LF 353 bi-fet op-amp.

given :- $A_V = 100$, $f_1 = 120\,Hz$, $f_2 = 5\,kHz$, $R_L = 2\,k\Omega$.

Sol :- For BiFet op-amp

choose $\boxed{R_2 = 1\,M\Omega}$

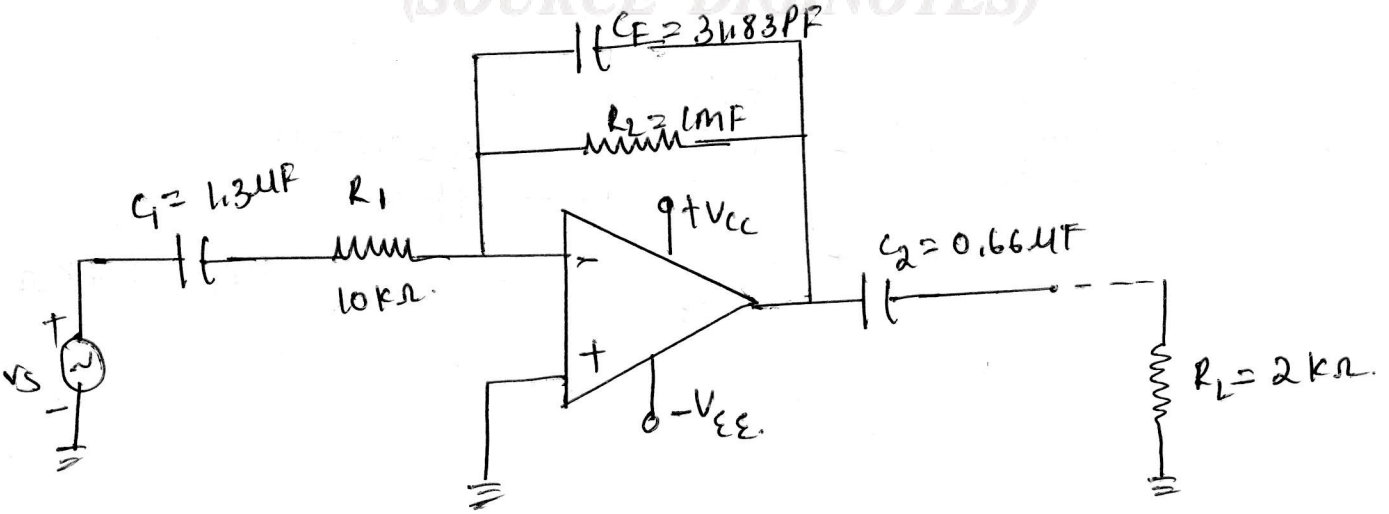
* W.K.T $A_V = \dfrac{R_2}{R_1}$ $\quad R_1 = \dfrac{R_2}{A_V} = \dfrac{1\,M\Omega}{100}$

$\boxed{R_1 = 10\,k\Omega}$

* $C_1 = \dfrac{1}{2\pi f_1 (R_1/10)} = \dfrac{1}{2\pi (120)(10k/10)} = C_1 = 1.32\,\mu F$

* $C_2 = \dfrac{1}{2\pi f_1 R_L} = \dfrac{1}{2\pi (120)(2k)} = 0.66\,\mu F$

* $C_F = \dfrac{1}{2\pi f_2 R_2} = \dfrac{1}{2\pi (5k)(1m)} = C_f = 31.83\,pF$



Voltage sources

Low resistance voltage source

A combination of voltage follower and a potential divider gives a low resistance voltage source. To increase the output current capacity a transistor is used at the output of the op-amp. The most of the op-Amp's have output current capacity of 25mA. Thus, using the transistor, this capacity can be increased to the maximum emitter current of the transistor. The base current of the transistor is very small and can easily be supplied by the op-amp.

The fig. 1 shows a low resistance voltage source using a transistor Q_1 at the output.

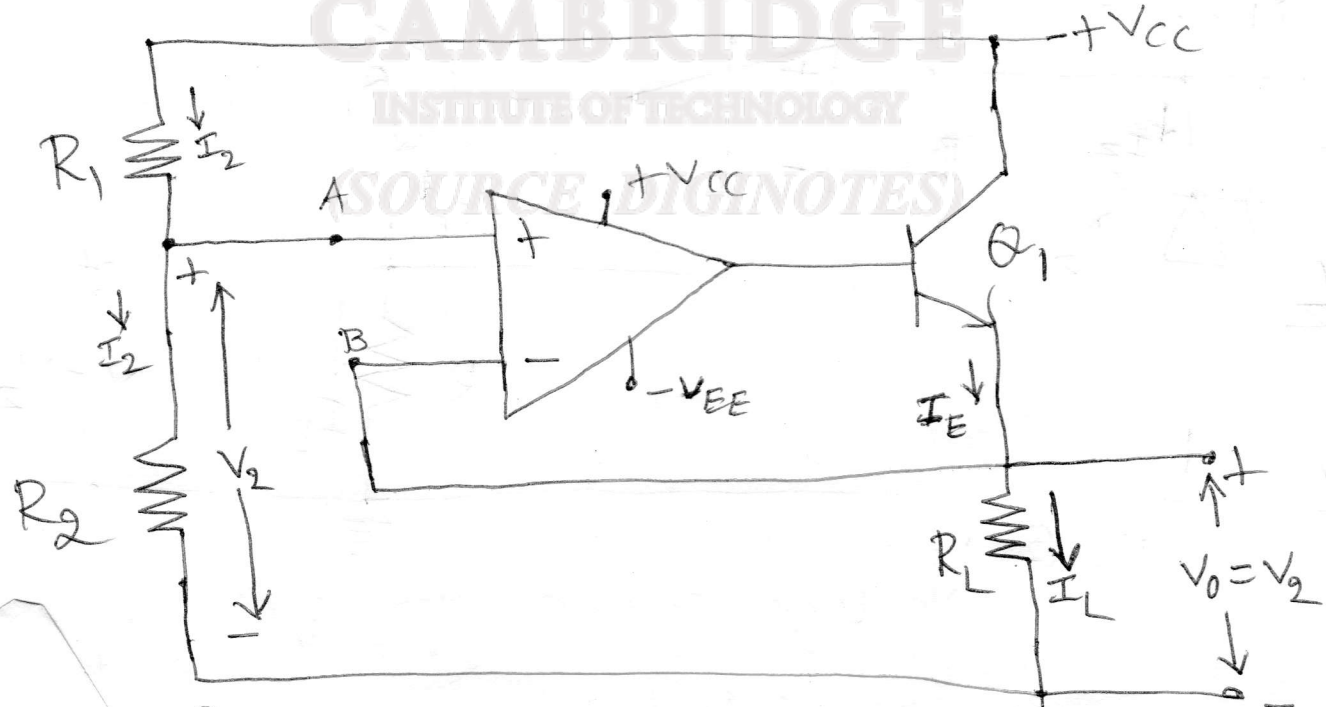


Fig. 1 Low resistance voltage source using potential divider. (or) Reference voltage derived from potential divider.

The node 'A' is at potential V_2 which is derived from $+V_{CC}$ with the help of potential divider R_1 and R_2. The node 'B' is also at potential V_2 which is derived from output (Emitter terminal of transistor Q_1). Therefore, $V_A = V_B = V_2$.
The V_B is nothing but the output voltage, as inverting terminal is connected to the emitter of the transistor. Thus, the output is maintained at V_2, which remains constant.
The disadvantage of this circuit is that if the supply voltage changes, the output voltage also changes. To avoid this limitation, a zener diode is used to generate the desired reference voltage. This is shown in fig. (2).

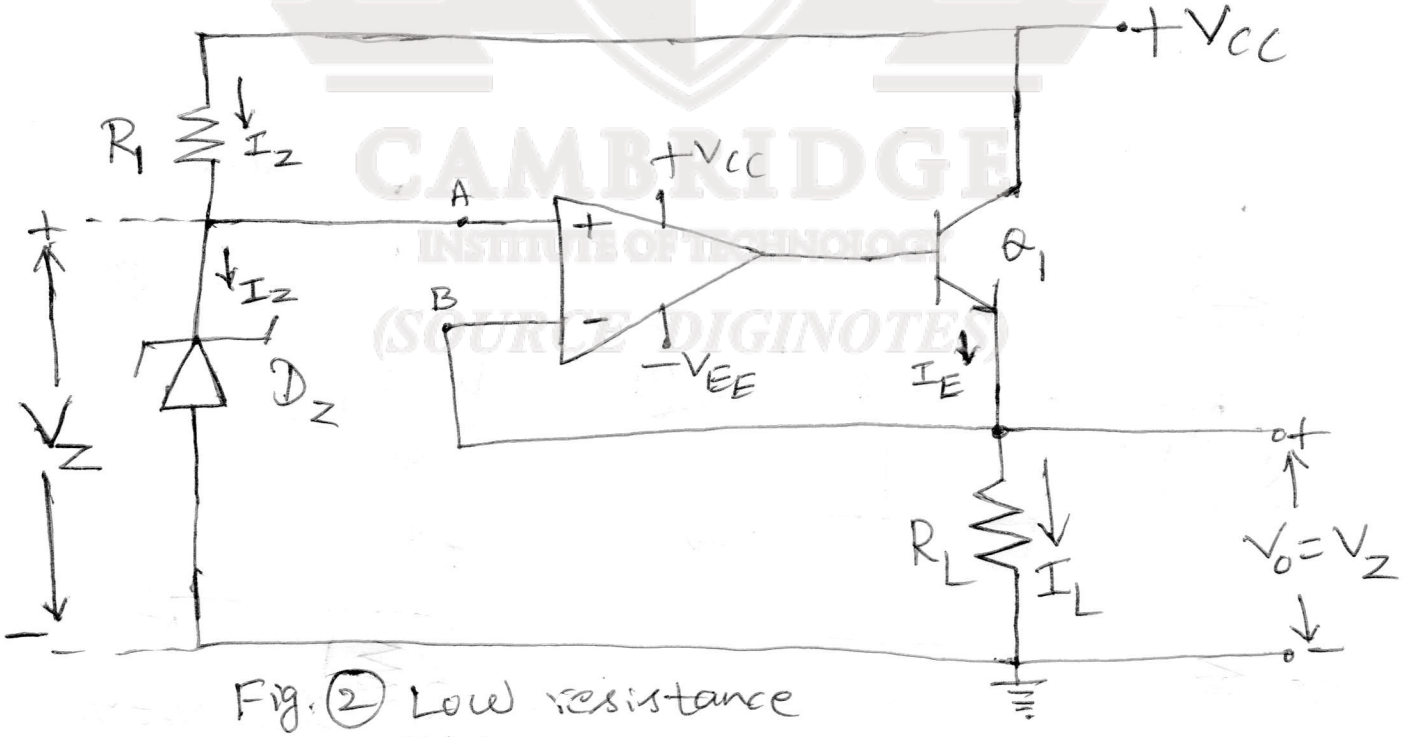


Fig. (2) Low resistance voltage source derived from Zener diod (or) Reference voltage derived from a Zener diode.

The resistance R_2 of the potential divider is replaced by a zener diode. The node 'A' is maintained at a potential V_2 due to the zener diode. The node 'B' is also maintained at a potential V_Z due to an inverting terminal is connected to emitter of the transistor Q_1. Therefore, $V_A = V_B = V_Z$. Hence the output V_0 is maintained constant at zener voltage V_Z.

Though there are supply voltage variations, I_Z gets adjusted, but the zener voltage V_Z approximately same. Thus the output approximately constant irrespective of supply voltage variations.

Design steps for the voltage source shown in fig. 1.

It is necessary to select a transistor which can handle a required load current. Then the the resistors R_1 and R_2 must be calculated in the usual way. Thus if 'I_2' is the potential divider current then,

$$R_2 = \frac{V_2}{I_2} = \frac{V_0}{I_2} \quad (\because V_0 = V_2 \text{ in the circuit shown in fig. 1})$$

But $I_2 = 100\, I_{B\,max} = 100 \times 500 \times 10^{-9}$

$= 50\,\mu A.$

for R_1: Applying KVL along the path $+V_{CC} \rightarrow R_1 \rightarrow R_2 \rightarrow GND$, we get,

$$V_{CC} - I_2R_1 - I_2R_2 = 0$$

$$V_{CC} - I_2R_1 - V_2 = 0$$

$$I_2R_1 = V_{CC} - V_2$$

$$\therefore \boxed{R_1 = \frac{V_{CC} - V_2}{I_2}} \quad \text{(OR)} \Rightarrow \boxed{R_1 = \frac{V_{CC} - V_0}{I_2}}$$

$\because V_0 = V_2$ in circuit shown in fig. (1)

Design steps for the circuit shown in fig (2).

First, select the zener diode with proper breakdown voltage and then find the value of R_1 by applying KVL along the path $+V_{CC} \rightarrow R_1 \rightarrow D_Z \rightarrow GND$,

i.e, $V_{CC} - I_ZR_1 - V_Z = 0$

$$I_ZR_1 = V_{CC} - V_Z$$

$$\therefore \boxed{R_1 = \frac{V_{CC} - V_Z}{I_Z}}$$

where, I_Z is zener diode current and it must be 20mA ($I_Z = 20$ mA) for the best stability for all the low current zener diodes.

Problems:

(1) Design a voltage source using a zener diode to provide approximately 6V output. The load resistance has a minimum value of 150Ω. The available supply voltage is ±12V.

Solution:

Given, $V_o = 6V$ and $R_{L(min)} = 150\Omega$.

Select a zener diode with a breakdown voltage of 6.3V.

A IN753 zener diode has $V_z = 6.3V$. ∴ use a IN753

The recommended current for the best stability for all low-current zener diodes is $\boxed{I_z = 20mA}$

∴ choose $\boxed{I_z = 20mA}$

$$\therefore R_1 = \frac{V_{cc} - V_z}{I_z} = \frac{12 - 6.3}{20 \times 10^{-3}} = 285\Omega$$

$$I_{L(max)} = \frac{V_o}{R_{L(min)}} = \frac{V_z}{R_{L(min)}} = \frac{6.3}{150} = 42mA$$

Transistor specification is,

npn device, $I_{E(max)} > 42mA$, $V_{CE(max)} > 12V$

op-amp specification is,

$V_{cc} = \pm 12V$,

the current gain (min) is

$$h_{fe(min)} = \frac{I_{L(max)}}{I_{o(max)}}$$

Generally, $I_{E(max)} > I_{L(max)}$ and $V_{CE(max)} > V_{cc}$ for transistor specification

where, $I_{L(max)}$ = max. current through load.

$I_{o(max)}$ = max. current at output of op-amp.

choose $h_{fe(min)} = 20$

$$\therefore I_{o(max)} = \frac{I_{L(max)}}{h_{fe(min)}} = \frac{42mA}{20} \simeq 2mA$$

Since the maximum current can be supplied by a 741-op-amp is 25 mA, 741 op-amp or LM 108 op-amp can be used.

(2) Design a voltage source using a zener diode to provide approximately 7V output. The minimum load resistance is 200Ω. The supply voltages are ±15V.

Ans: $R_1 = 375\,\Omega$

$I_{L(max)} = 37.5\,mA$

$I_{O(max)} = 1.875\,mA$

NOTE: Choose $I_{E(max)} > I_{L(max)}$ and $V_{(E_{max})} > V_{CC}$

Precision voltage source

In case of zener diode voltage source, the zener voltage can vary little bit as zener current changes due to changes in the power supply voltage. Hence in a precision voltage source an arrangement is used which maintains the output voltage constant. In this type of voltage source, in addition to resistor R_1 and zener diode, a potential divider using the resistors R_2 and R_3 is also used. Both these circuits are supplied from the output terminal of the op-Amp, instead of Vcc. This is shown in fig. (3).

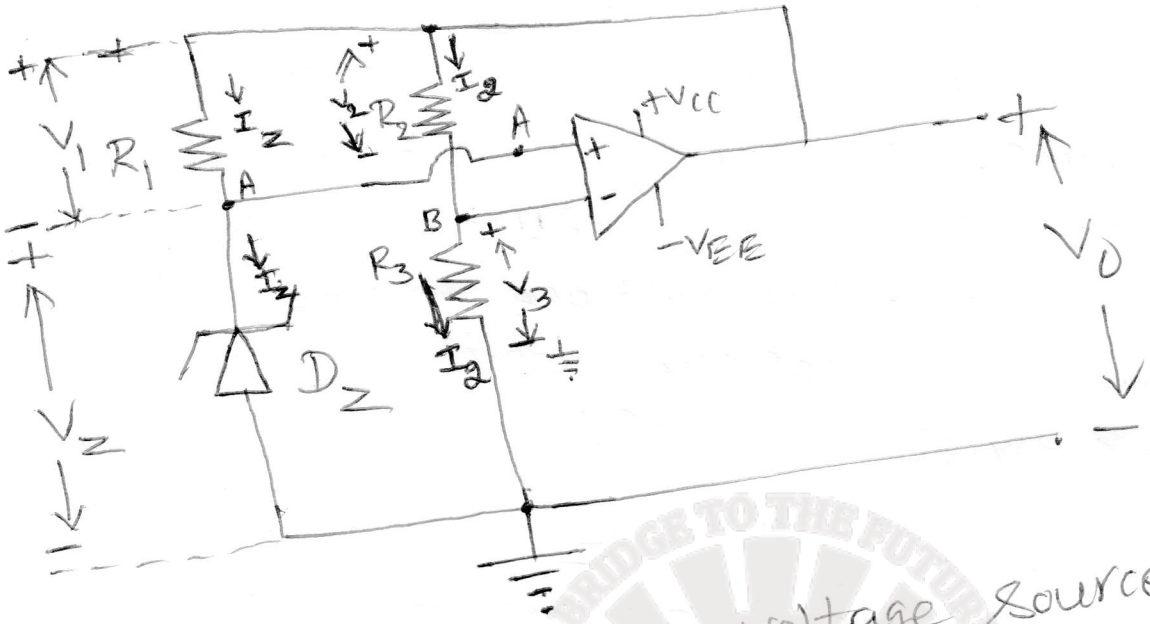


Fig. 3 precision voltage source.

If the output current requirement is large, a transistor can be used at the output of the op-amp.

The node 'A' is at potential V_z. The node 'B' is also at the same ~~potent~~ potential, i.e, $V_A = V_B = V_z$. Thus the drop across R_3 i.e, $V_3 = V_{R_3} = V_z$. Hence the drop across ~~R3~~ R_2 is $V_2 = V_1$ [(R_1, D_z) and (R_2, R_3) are in parallel]. while the output voltage is $V_0 = V_1 + V_z$ if R_1 and D_z circuit is considered.

The output voltage is ~~$V_0 = V_2 + V_3$~~ $V_0 = V_2 + V_3$ if R_1 an R_2 circuit is considered.

Now, if the output voltage increases by ΔV_0 then the current I_2 increases. Hence the drop V_3 increases by ΔV_3.

$$\therefore \Delta V_3 = \frac{\Delta V_0 \times R_3}{R_2 + R_3}$$

As the voltage of inverting input terminal increases, the output tends to move in negative direction. Thus the output decreases to compensate the initial increase. Similarly, if V_0 decreases, then V_3 also decreases due to reduction in the current I_2. This drop in the voltage at the inverting input terminal, causes the output to increase back to it's original value.

Relation between V_0 and V_Z

Note that $V_3 = V_Z$ and $V_0 = V_1 + V_Z = V_2 + V_3$

$$\therefore I_2 = \frac{V_3}{R_3} = \frac{V_Z}{R_3} \quad \text{--- (1)}$$

and $V_0 = V_2 + V_3$

$$= I_2 R_2 + I_2 R_3$$

$$V_0 = I_2 (R_2 + R_3) \quad \text{--- (2)}$$

Substitute eqn (1) in (2)

$$\therefore \boxed{V_0 = \frac{V_Z}{R_3}(R_2 + R_3)} \quad \text{--- (3)}$$

Equation (3) tells that, the desired output voltage is not only depending on V_Z, but also on the selection of R_2 and R_3.

Practically there is ±5% to ±10% tolerance in zener voltage, hence a potentiometer is introduced in series with R_3 for the proper and precise adjustment of output. This is shown in fig. (4).

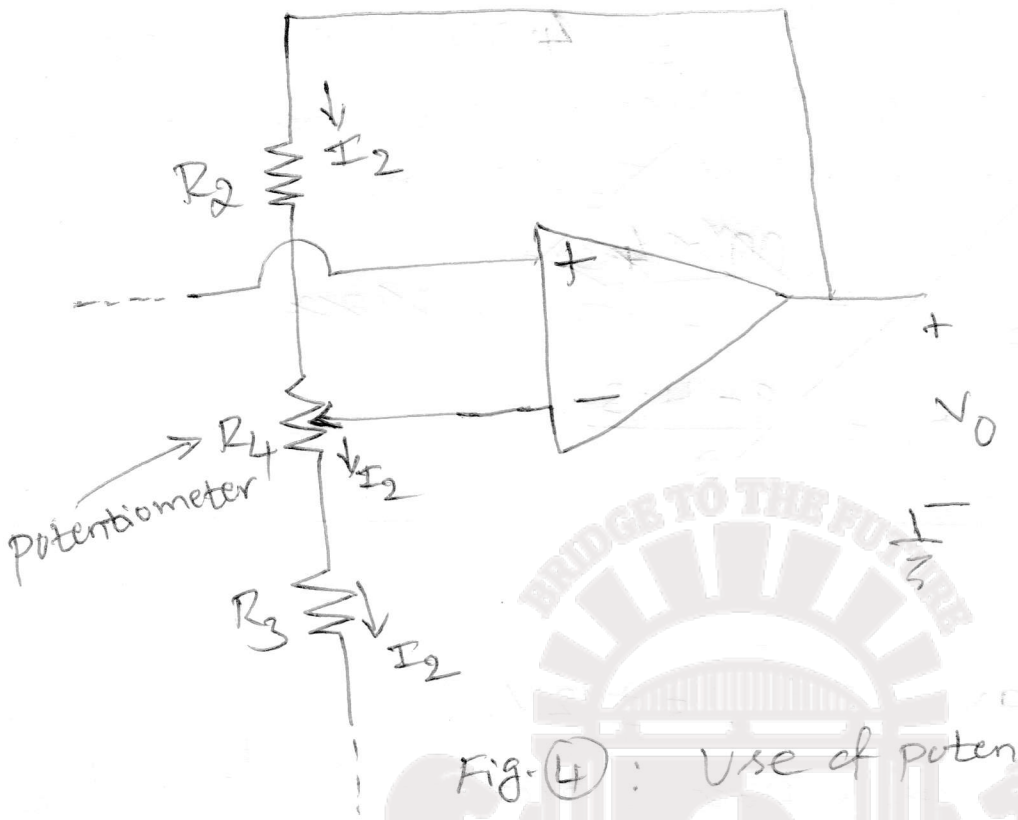


Fig. 4 : Use of potentiometer.

Design steps for precision voltage source

1. Zener diode is selected first with V_z equal to half the output voltage ie, $V_z = \frac{V_0}{2}$.
2. Then the resistance R_1 in series with zener diode (D_z) is calculated.
3. Then the potential divider resistor values are determined in the usual way.

The potential divider current is assumed to 100 times more than the maximum biasing current of the op-amp. ie, $I_2 = 100 I_{B\,max}$.

Problems :

1. Design a precision voltage source to provide an output of 9V. The available supply is ±12V. Allow for approximately ±10% tolerance on the zener diode voltage.

~~Solution~~ :

~~A IN749 zener diode has $V_Z = 4.3V$. Use a IN753. The recommended current for best voltage stability for low-current zener diodes is $I_Z = 20mA$.~~

$$\cancel{R_1 = \frac{V_o - V_Z}{I_Z} = \frac{9V - 4.3V}{20mA} = 285\Omega}$$

$$\cancel{I_{L(max)} = R_1 = \frac{9 - 4.3}{20}}$$

Solution

$V_o = 9V$, supply $= \pm 12V$.

Select zener with voltage approximately half the output voltage.

$$\therefore V_Z \simeq \frac{V_o}{2} \simeq \frac{9}{2} \simeq 4.5V$$

Use a IN749 which has $\boxed{V_Z = 4.3V.}$

$$\therefore R_1 = \frac{V_o - V_Z}{I_Z} = \frac{9 - 4.3}{20 \times 10^{-3}}$$

$$\boxed{R_1 = 235\Omega}$$

For R_2, R_3, and R_4,

Using a 741 op-amp,

Let, $I_2 \simeq 100\, I_{B(max)} = 100 \times 500nA = 50\mu A$

Provide a potentiometer R_4 for $\pm 10\%$ tolerance on the zener diode voltage.

$$\therefore R_3 + R_4 = \frac{V_Z + 10\% \text{ of } V_Z}{I_2}$$

$$R_3 + R_4 = \frac{4.3 + \frac{10}{100} \times 4.3}{50 \times 10^{-6}}$$

$$\boxed{R_3 + R_4 = 94.6\,k\Omega}$$

and $R_4 = 20\%$ of $(R_3 + R_4)$ i.e,

$$R_4 = \frac{20}{100} \times 94.6\,k\Omega$$

$\therefore R_4 = 18.9\,k\Omega$ (potentiometer) variable

$$\therefore R_3 = (R_3 + R_4) - R_4$$
$$= 94.6\,k\Omega - 18.9\,k\Omega$$

$\boxed{R_3 = 75.7\,k\Omega}$ ~~stands~~ fixed

$$\therefore I_2 = \frac{V_Z + 10\% \text{ of } V_Z}{R_3 + R_4} = \frac{4.3 + \frac{10}{100} \times 4.3}{75.7k + 18.9k}$$

$\therefore I_2 = 50\,\mu A$.

$$\therefore R_2 = \frac{V_0 - (V_{R_3} + V_{R_4})}{I_2}$$

where, V_{R_3} and V_{R_4} are the voltage drops across the resistors R_3 and R_4 respectively in circuit shown in fig. (4).

$$R_2 = \frac{9 - (4.3 + 10\% \text{ of } V_Z)}{50\mu A}$$

$$R_2 = \frac{9 - (4.3 + \frac{10}{100} \times 4.3)}{50\mu A}$$

$$\therefore \boxed{R_2 = 85.4\,k\Omega}$$

~~Answer~~

(2) Design a precision voltage source to provide the output of 12V. The available supply is ±15V. Provide the arrangement considering ±5% tolerance of zener diode voltage.

Solution Choose $V_Z = \frac{V_o}{2} = 6V$

∴ select 6.3V zener diode such as IN753.

Ans: ∴ $R_1 = 285\Omega$

$R_3 + R_4 = 132.3k\Omega$

Let R_4 be 10% of $R_3 + R_4$

∴ $R_4 = 13.23k\Omega$

∴ $R_3 = 119.07k\Omega$

∴ $R_2 \simeq 110k\Omega$

Current source

A circuit which supplies a constant current in the conventional direction from positive to negative is called a current source.

Fig (1) shows a current source with a floating load.

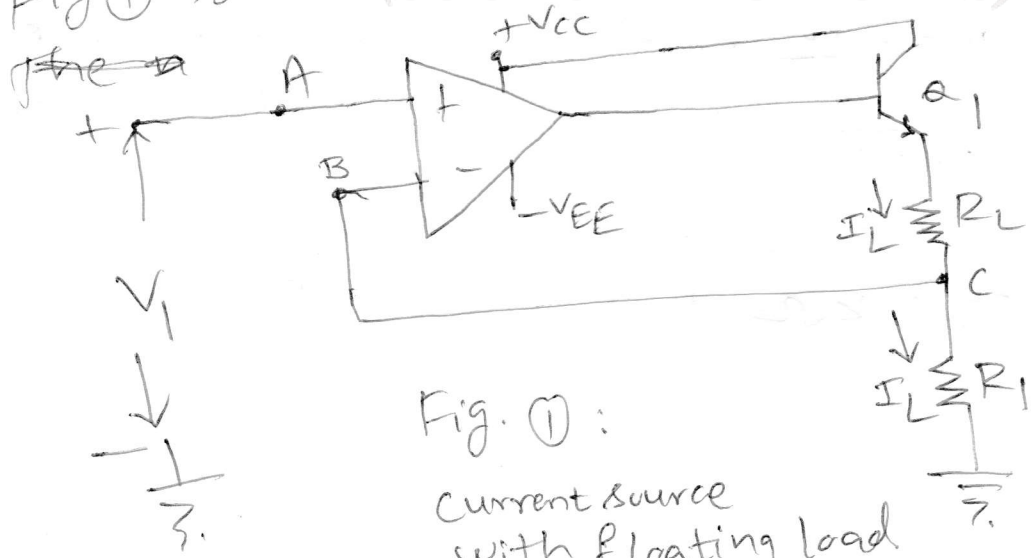


Fig. (1): Current source with floating load

The node 'A' is at potential V_1. Thus, the node 'B' is also at potential V_1, i.e, $V_A = V_B = V_1 = V_C$

$$\therefore I_L = \frac{V_B}{R_1} = \frac{V_1}{R_1} \quad \Big| \because V_C = V_B = V_A.$$

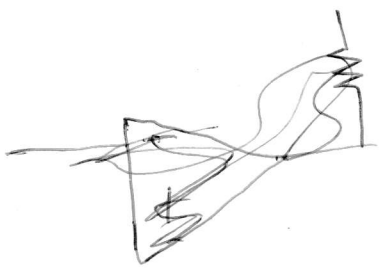
$$\therefore \boxed{I_L \propto V_1}$$

The negative feedback is used to maintain the load current is always proportional to the input voltage. The proportionality constant is generally $\frac{1}{R_1}$. Hence this circuit is also called transconductance amplifier. It is also called a voltage controlled current source.

The expression $I_L = \frac{V_1}{R_1}$ holds regardless of the type of the load. No matter what the load is, the op-amp will draw the current I_L whose magnitude depends only on V_1 and R_1.

The transistor may not be used if the maximum load current is less than 25 mA.

When one terminal of the load is grounded, then it is ~~called~~ not possible to place the load within the feedback loop. Such a current source is called current source with grounded load. The fig (2) shows a current source with grounded load.



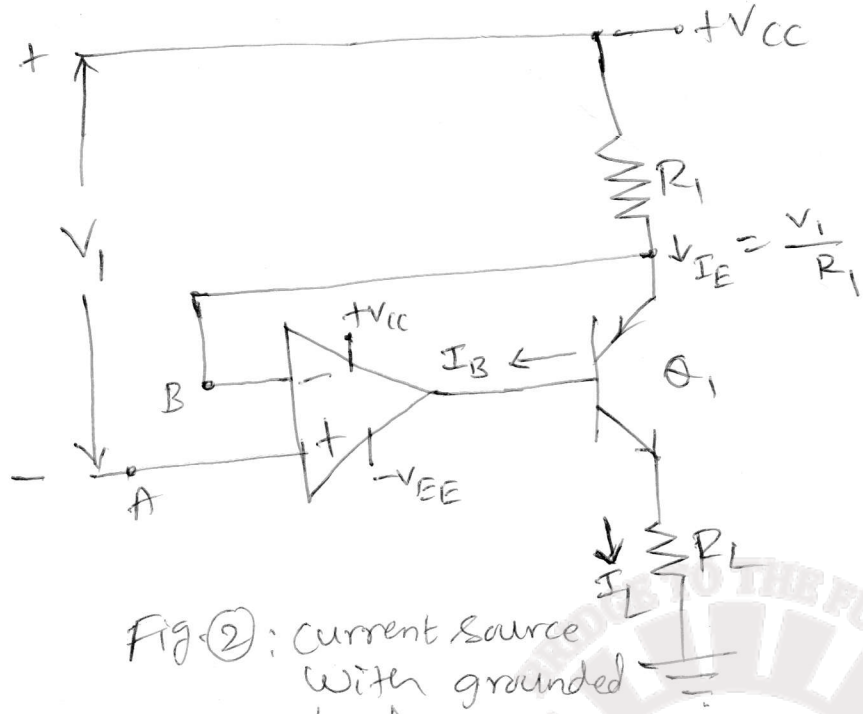


Fig ②: current source with grounded load.

A pnp transistor is used in this circuit. The emitter of the transistor Q_1 is connected to the inverting terminal of the op-amp. The potential present at nodes 'A' and 'B' is V_1 i.e, $V_A = V_B = V_1$. Hence across R_1, the voltage V_1 appears. ~~As the~~ The current through R_1 is I_E.

$$\therefore I_E = \frac{V_1}{R_1} = \text{constant}$$

and

$$I_E = I_B + I_L$$

$$\therefore \boxed{I_L = I_E - I_B}$$

Due to base current of transistor, I_L is slightly different than the emitter current I_E. This limitation can be eliminated by a p-channel FET. The drain and source currents are equal hence the load current is almost same as the current through R_1 as shown in fig ③. If the load current is high, power MOSFET can be used. The current source using MOSFET is shown in fig ④.

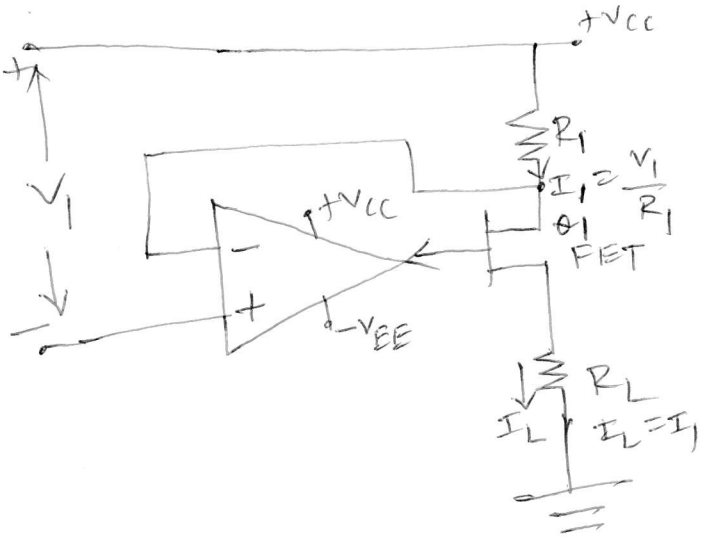


Fig. (3) : current source using FET

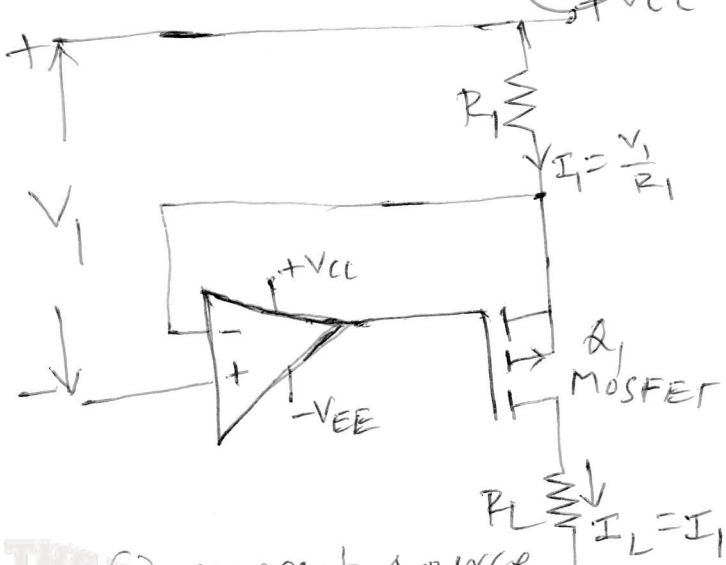


Fig. (4) current source using MOSFET.

In designing such current sources following points must be noted.

(1) For BJT (current sources) circuits with grounded load, the drop across R_L makes collector voltage above ground level. Hence allowing the collector-emitter voltage of 3V, the emitter of the transistor must be atleast $I_L R_L + 3V$ above the ground level.

(2) For FET current sources, the drain-source voltage of FET should be about 1V higher than maximum pinch-off voltage.

$$\therefore V_{DS(min)} = V_{GS(off)} + 1V$$

(3) For MOSFET current sources, V_{DS} should be about 1V higher than the voltage due to the drain current and drain-source ON resistance.

$$\therefore V_{DS(min)} = I_D R_{D(on)} + 1V.$$

Current Sinks

Two current sink circuits are illustrated in Figs. 6-5(a) and (b). These are similar to the current sources in Figs. 6-3(b) and 6-4(b) except that an *npn* bipolar transistor and an *n*-channel MOSFET are now used. The operation of the circuits and the design approach for each is the same as for the current source circuits.

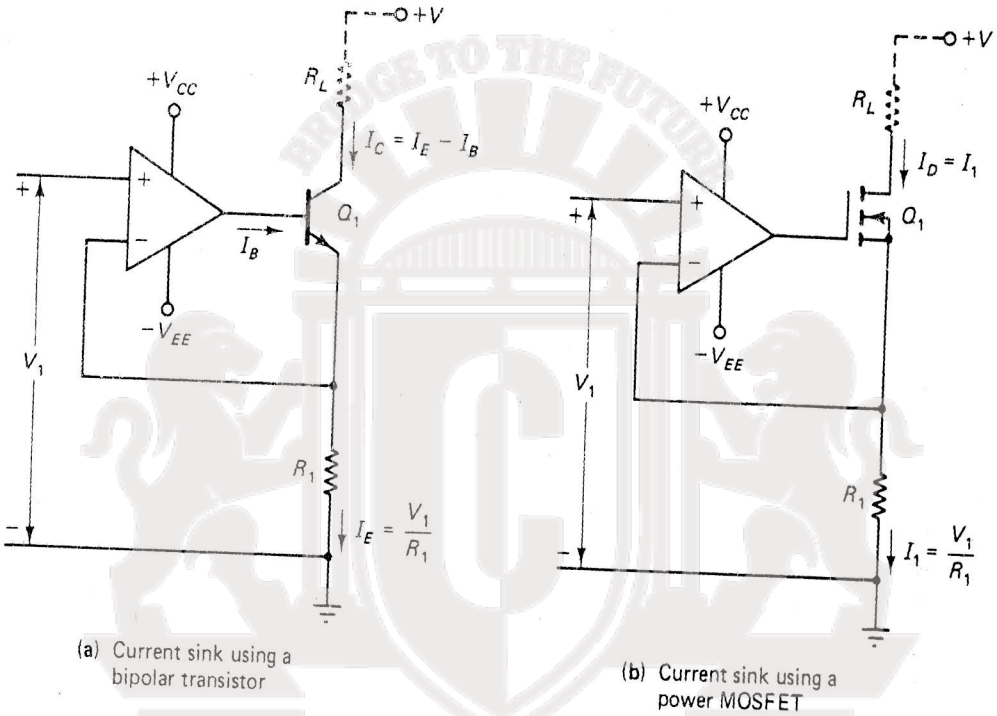


Figure 6-5 A current sink circuit using a bipolar transistor has a constant sink current because the emitter current is held at V_1/R_1. Use of a MOSFET (or a FET) gives a sink current precisely equal to the current through R_1.

6-3 PRECISION CURRENT SINK AND SOURCE CIRCUITS

The precision current sink circuit in Fig. 6-6 is the same as the precision voltage source in Fig. 6-2 except that an *n*-channel power MOSFET (Q_1) has been added at the op-amp output. A constant voltage is maintained at the output as explained in Section 6-1. In the case of Fig. 6-6, the output voltage at the source terminal of the FET is held constant. Thus, the current through R_5 is held constant and the MOSFET drain current is a constant quantity.

The current source circuit in Fig. 6-7 is a modified form of the circuit in Fig. 6-6. A *p*-channel MOSFET is used for Q_1 and components D_1 and R_1 have been interchanged in order to maintain a constant voltage across R_5 in its new position. Thus, once again, the drain current of the MOSFET is held constant.

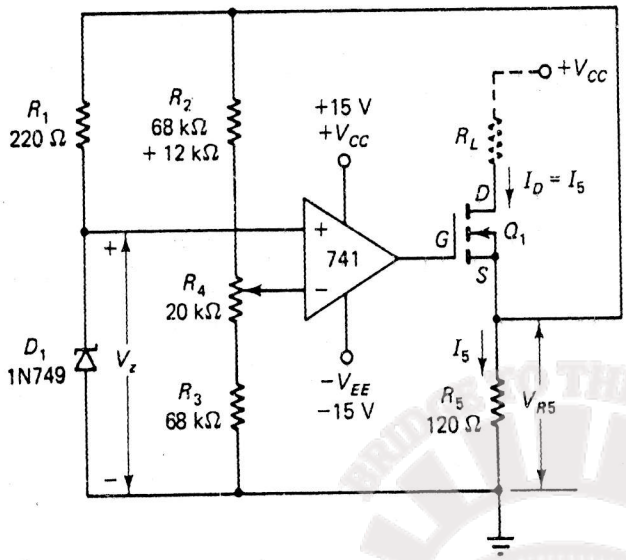


Figure 6-6 Precision current sink using a precision voltage source and a power MOSFET.

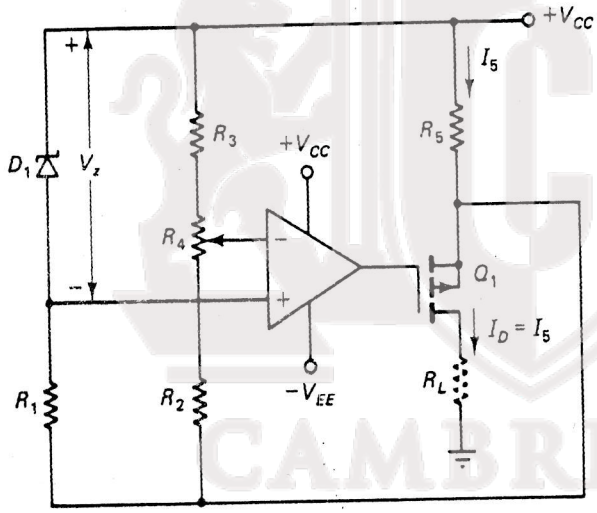


Figure 6-7 Precision current source using a precision voltage source and a power MOSFET.

To design a precision current source or sink circuit, the voltage drop across R_5 is first determined in the same way as V_{R1} is calculated in Example 6-3. Then the rest of the circuit is designed as for the precision voltage source in Example 6-2.

Example 6-4

Design a precision current sink, as in Fig. 6-6, to provide 75 mA through a load which has a maximum resistance of 50 Ω. The supply voltage is ±15 V and a 741 op-amp is to be used.

Solution

For the MOSFET, $V_{DS(max)} = V_{CC} = 15$ V

and $I_{D(max)} = I_L = 75$ mA

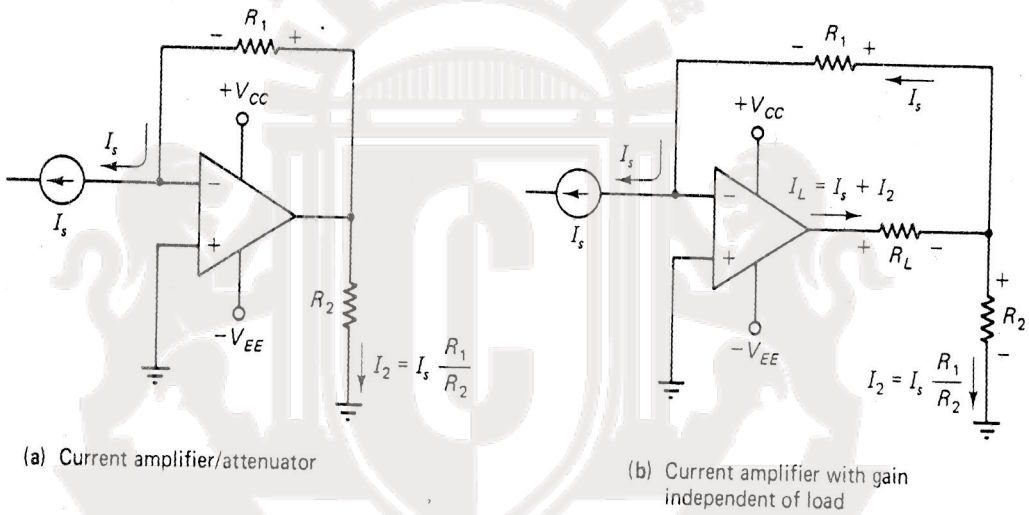
voltage drop $-I_sR_1$, which is also the negative voltage at op-amp output. If the current direction is reversed, the output voltage becomes positive.

Current Amplifier

In Fig. 6-9(a), resistor R_2 has been added to the circuit of Fig. 6-8. The current through R_2 is

$$I_2 = \frac{V_o}{R_2} = \frac{I_sR_1}{R_2}$$

So, the output current is R_1/R_2 times the input current and the circuit is a current amplifier if $R_1 > R_2$. Where $R_2 > R_1$, the circuit is a current attenuator.



(a) Current amplifier/attenuator

(b) Current amplifier with gain independent of load

Figure 6-9 Current amplifier/attenuator circuits with grounded and floating loads. For the grounded load circuit, the current gain depends upon the resistance of load R_2. For the floating load circuit, the gain is independent of the load resistance.

One disadvantage of the circuit in Fig. 6-9(a) is that the current gain/attenuation is dependent on the resistance of R_2, which is the load resistance. If the load can be floating (ungrounded), then the circuit shown in Fig. 6-9(b) can be used. Here, the load current is

$$I_L = I_s + I_2$$

$$= I_s + I_s\frac{R_1}{R_2}$$

or

$$I_L = I_s\left(1 + \frac{R_1}{R_2}\right) \tag{6-4}$$

Note that the resistance of the load is not involved in Eq. 6-4. So, the circuit of Fig. 6-9(b) operates as a current amplifier with a gain which is independent of the load resistance. Of course the voltage drop across the load must not be so large that the op-amp output attempts to exceed its maximum output voltage range.

The VN2222L n-channel power MOSFET has $V_{DS(max)} = 60$ V, $I_{D(max)} = 150$ mA, and $R_{D(on)} = 7.5\ \Omega$. So, the VN2222L is a suitable device for Q_1.

$$V_{L(max)} = I_L \times R_{L(max)} = 75\text{ mA} \times 50\ \Omega$$
$$= 3.75\text{ V}$$

For satisfactory operation of Q_1,

let $$V_{DS(min)} = (I_D R_{D(on)}) + 1\text{ V} = (75\text{ mA} \times 7.5\ \Omega) + 1\text{ V}$$
$$\approx 1.6\text{ V}$$

and $$V_{R5(max)} = V_{CC} - V_{L(max)} - V_{DS(min)}$$
$$= 15\text{ V} - 3.75\text{ V} - 1.6\text{ V}$$
$$\approx 9.6\text{ V}$$

$$R_5 = \frac{V_{R5}}{I_L} = \frac{9.6\text{ V}}{75\text{ mA}}$$
$$= 128\ \Omega$$

Use $R_5 = 120\ \Omega$. Then,

$$V_{R5} = I_L \times R_5 = 75\text{ mA} \times 120\ \Omega$$
$$= 9\text{ V}$$

The circuit in Example 6-2 was designed for $V_o = 9$ V. So, the remaining component calculations for the current sink are exactly as for Example 6-2.

6-4 CURRENT AMPLIFIERS

Current-to-Voltage Converter

The current-to-voltage converter circuit in Fig. 6-8 can be thought of as an inverting amplifier without an input resistor. Because the op-amp noninverting input terminal is grounded, the inverting input remains at ground level. So, the input current source is effectively short-circuited to ground. With I_s much larger than the input bias current of the op-amp, virtually all of I_s flows through resistor R_1 to produce a

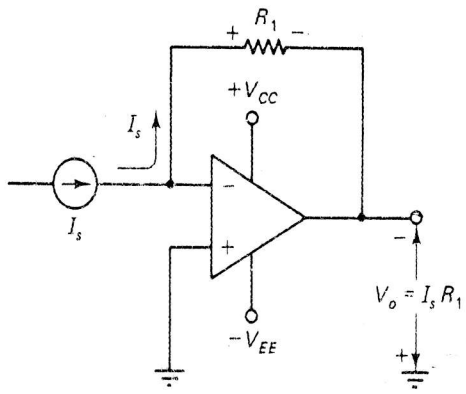


Figure 6-8 Current-to-voltage converter circuit which behaves like an inverting amplifier without an input resistor.

Potential Divider

$$I_1 \gg (I_{B(\max)} \text{ for } A_1)$$

let

$$I_1 = 50\ \mu\text{A}$$

$$V_{(R1+R2)} \approx V_{R4} + 10\% = 10\text{ V} + 10\%$$

$$= 11\text{ V}$$

$$R_1 + R_2 = \frac{11\text{ V}}{50\ \mu\text{A}} = 220\text{ k}\Omega$$

$R_2 = 20\%$ of $(R_1 + R_2) = 44\text{ k}\Omega$ (use 50 kΩ standard value potentiometer)

$R_1 = (R_1 + R_2) - R_2 = 220\text{ k}\Omega - 50\text{ k}\Omega$

$= 170\text{ k}\Omega$ (use 150 kΩ standard value, and recalculate I_1)

$$I_1 = \frac{V_{(R1+R2)}}{R_1 + R_2} = \frac{11\text{ V}}{(150\text{ k}\Omega + 50\text{ k}\Omega)}$$

$$= 55\ \mu\text{A}$$

$$R_3 = \frac{V_{CC} - V_{(R1+R2)}}{I_1} = \frac{18\text{ V} - 11\text{ V}}{55\ \mu\text{A}}$$

$= 127\text{ k}\Omega$ (use 120 kΩ standard value)

6-8 INSTRUMENTATION AMPLIFIER

Differential Input/Output Amplifier

Figure 6-13 shows the circuit of an amplifier which accepts a differential input voltage and produces a differential output. As will be explained, this circuit has certain advantages over the difference amplifier introduced in Section 3-6. To understand the operation of the differential input/output amplifier, assume for the moment that the junction of resistors R_2 and R_3 in Fig. 6-13 is grounded. Op-amp A_1 together with resistors R_1 and R_2 would function as a noninverting amplifier. The input voltage to A_1 would be developed across R_2 and the voltage gain would be $(R_1 + R_2)/R_2$. Similarly, if the junction of resistors R_1 and R_2 was grounded, op-amp A_2 and resistors R_2 and R_3 would behave as a noninverting amplifier with a voltage gain of $(R_2 + R_3)/R_2$.

Now consider the operation of the complete circuit. Because of the noninverting amplifier configuration of A_1 and A_2 and the resistors, the voltage at the junction of R_1 and R_2 is equal to input voltage v_1. Also, the voltage at the junction of R_2 and R_3 equals input voltage v_2. Consequently, the voltage across resistor R_2 is

$$V_{R2} = v_1 - v_2 = V_i \text{ (the differential input)}$$

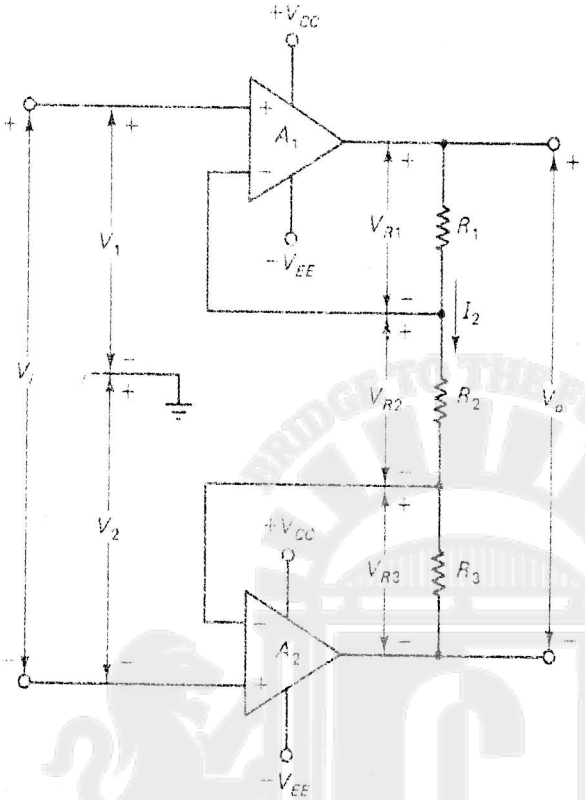


Figure 6-13 Differential input/output amplifier which accepts a differential input voltage and amplifies it to produce a differential output. With $R_3 = R_1$, the voltage gain is $A_v = (2R_1 + R_2)/R_2$.

This gives the current through R_2 as

$$I_2 = \frac{V_i}{R_2}$$

The differential output voltage is,

$$\begin{aligned} v_o &= V_{R1} + V_{R2} + V_{R3} \\ &= I_2(R_1 + R_2 + R_3) \\ &= \frac{V_i}{R_2}(R_1 + R_2 + R_3) \end{aligned}$$

The circuit differential voltage gain is,

$$A_{v(\text{dif})} = \frac{V_o}{V_i} = \frac{R_1 + R_2 + R_3}{R_2} \tag{6-5}$$

Normally $R_1 = R_3$

so,

$$A_{v(\text{dif})} = \frac{2R_1 + R_2}{R_2} \tag{6-6}$$

Note that the voltage gain can be altered by adjusting a single resistor; R_2.

Like all amplifiers with a differential input, the common mode gain of the differential input/output amplifier is an important quantity. Suppose the two inputs are connected together and a common mode noise voltage (V_n) is applied to the two as

shown in Fig. 6-14. The junction of R_1 and R_2 will be at the same voltage as the noninverting input terminal of A_1, and the junction of R_2 and R_3 will be at the same voltage as the noninverting input of A_2. That is, both resistor junctions will be at v_n volts with respect to ground. There will be no current flow through R_1, R_2, or R_3, and the output voltage of each amplifier will be v_n volts. This means the common mode gain is

$$A_{v(cm)} = 1 \tag{6-7}$$

So, common mode signals will be passed through but not amplified by the differential input/output amplifier.

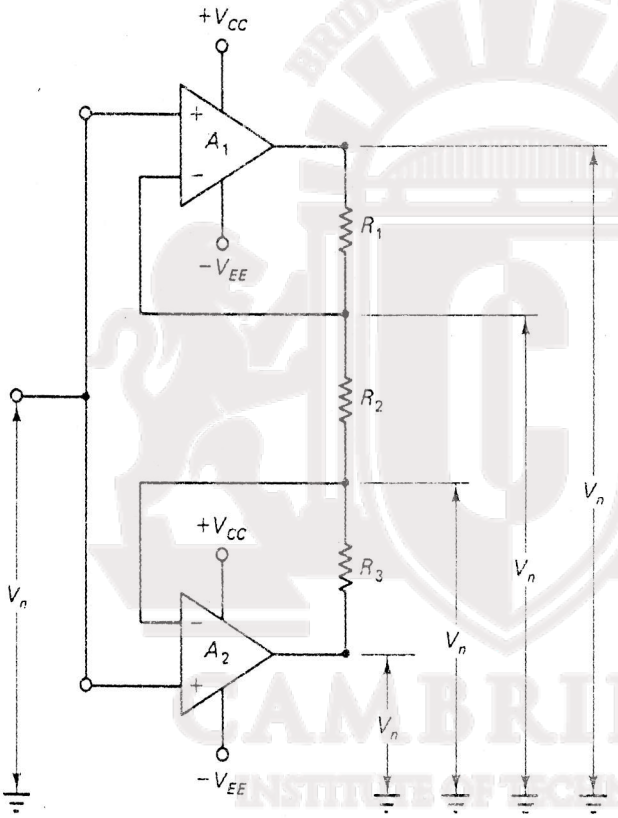


Figure 6-14 A common mode voltage applied to a differential input/output amplifier is reproduced at the output. $A_{v(cm)} = 1$.

The differential input/output amplifier is normally used in conjunction with the difference amplifier discussed in Section 3-6. The two circuits are reproduced in Fig. 6-15 for comparison. The resistance at each input terminal of the differential input/output amplifier is extremely high because of the noninverting amplifier configuration. The input resistance of the difference amplifier is $R_i = R_1$ at input terminal 1, and $R_i = (R_3 + R_4)$ at terminal 2. The voltage gain of the differential input/output amplifier can be changed by adjusting only one resistor: R_2. Changing the gain of the difference amplifier requires that R_2 and R_4 be adjusted together to maintain equal amplification of both inputs. The common mode gain of the differential input/output amplifier is 1, compared to a common mode gain of zero for the difference amplifier. As illustrated in Fig. 6-15, the differential input/output amplifier operates with a floating load, while the difference amplifier uses a grounded load.

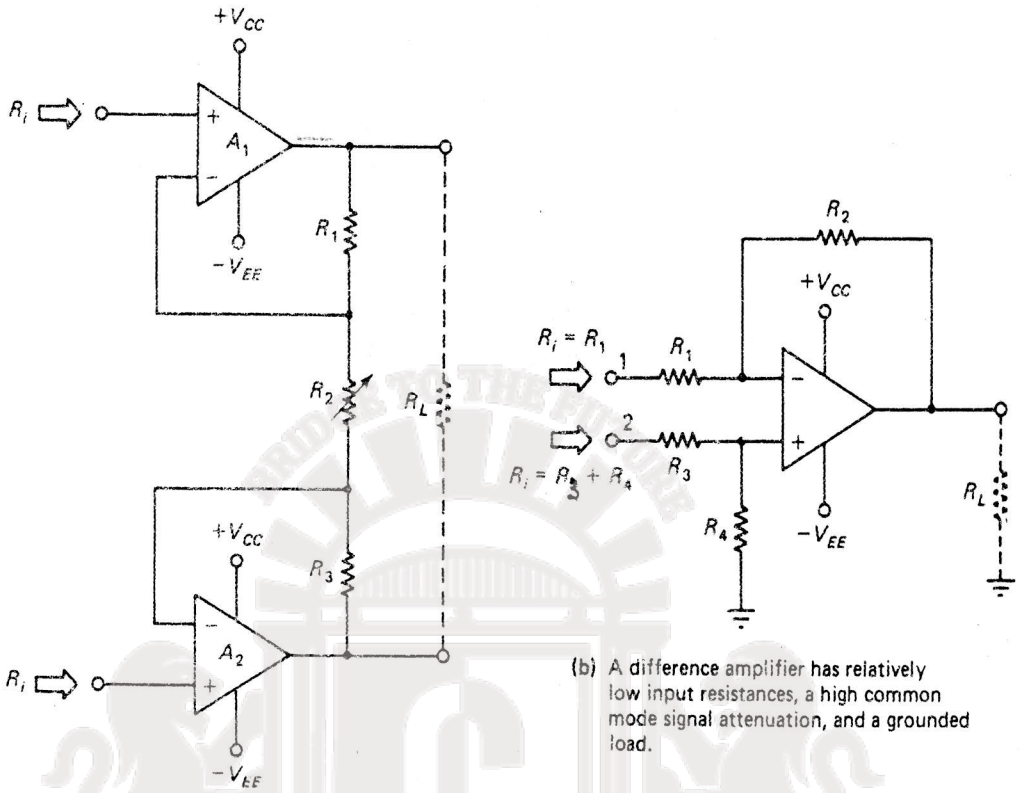


Figure 6-15 Comparison of a differential input/output amplifier and a difference amplifier.

Instrumentation Amplifier Circuit

The instrumentation amplifier circuit shown in Fig. 6-16 is a combination of the differential input/output amplifier (stage 1) and the difference amplifier (stage 2). The difference amplifier uses the differential output voltages from the differential input/output amplifier to drive a grounded load, as illustrated. For instrumentation purposes, most loads have one grounded terminal, otherwise ground loops and static electricity could cause problems. So, the ability to drive a grounded load is necessary. The differential input/output stage offers a very high input resistance at each input terminal. The voltage gain of the complete circuit is,

$$A_v = A_{v1} \times A_{v2}$$

where A_{v1} is the voltage gain of stage 1 and A_{v2} is the stage 2 gain.

$$A_v = \frac{2R_1 + R_2}{R_2} \times \frac{R_5}{R_4} \tag{6-8}$$

The overall voltage gain can be controlled by adjustment of R_2. The common mode signal attenuation for the instrumentation amplifier is that provided by the difference amplifier. As discussed in Section 3-6, this can be maximized by making resistor R_7

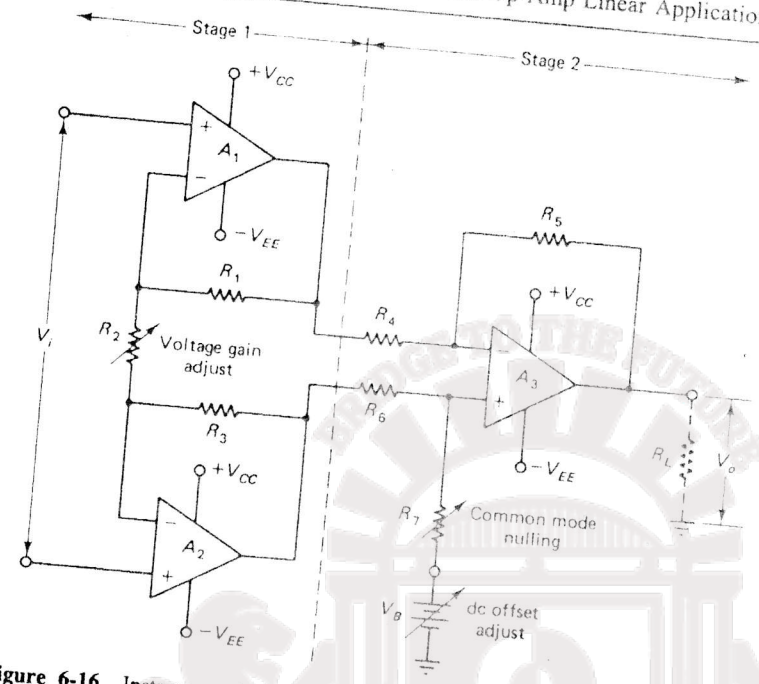


Figure 6-16 Instrumentation amplifier consisting of a differential input/output amplifier input stage and a difference amplifier output stage. The circuit has adjustable voltage gain, common mode output nulling, and dc output voltage level shifting.

adjustable. Also, as discussed in Section 3-6, the dc output voltage level can be controlled if R_7 is connected to an adjustable bias voltage instead of being directly grounded.

Example 6-7

Design an instrumentation amplifier to have an overall voltage gain of 900. The input signal amplitude is 15 mV, 741 op-amps are to be used, and the supply is ±15 V.

Solution

Stage 1

$$\text{let } A_{v1} \approx A_{v2} = \sqrt{A_v} = \sqrt{900} = 30$$

let

$$I_2 \gg I_{B(\max)}$$

$$I_2 = 100 I_{B(\max)} = 50\ \mu\text{A}$$

$$R_2 = \frac{V_i}{I_2} = \frac{15\ \text{mV}}{50\ \mu\text{A}} = 300\ \Omega \qquad \text{(use 500 } \Omega \text{ variable)}$$

Eq. 6-6,

$$A_{v(\text{dif})} = \frac{2R_1 + R_2}{R_2}$$

which gives, $R_1 = \frac{R_2}{2}[A_{v(dif)} - 1] = \frac{270\ \Omega}{2}[30 - 1]$

$\approx 3.9\ \text{k}\Omega$ (standard value)

$R_3 = R_1 = 3.9\ \text{k}\Omega$

Stage 2

$V_o = A_v V_i = 900 \times 15\ \text{mV}$

$= 13.5\ \text{V}$

$I_{S(min)} \gg I_{B(max)}$

let $I_S = 100 I_{B(max)} = 50\ \mu\text{A}$

$R_5 = \frac{V_o}{I_S} = \frac{13.5\ \text{V}}{50\ \mu\text{A}}$

$= 270\ \text{k}\Omega$ (standard value)

$R_4 = \frac{R_5}{A_{v2}} = \frac{270\ \text{k}\Omega}{30}$

$= 9\ \text{k}\Omega$ (use $8.2\ \text{k}\Omega + 820\ \Omega$ or $9.1\ \text{k}\Omega \pm 5\%$

$R_6 = R_4 = 9\ \text{k}\Omega$

$R_7 = R_5 \pm 20\% = 270\ \text{k}\Omega \pm 20\%$

$\approx 216\ \text{k}\Omega$ to $324\ \text{k}\Omega$ (use a $220\ \text{k}\Omega$ fixed resistor and a $100\ \text{k}\Omega$ variable)

Integrated Circuit Instrumentation Amplifier

Instrumentation amplifiers are available in a single integrated circuit package. I
6-17 shows the simplified circuit of the LH0036 IC instrumentation amplifier.
circuit, difference amplifier resistors R_3, R_4, R_5, and R_6 are all equal value co
nents; so that the voltage gain of that stage is 1. The overall voltage gain for th
cuit is set by the externally connected resistor R_G. The equation for voltage g
similar to Eq. 6-6.

$$A_v = \frac{2R_1 + R_G}{R_G}$$

With $R_1 = R_2 = 25\ \text{k}\Omega$, the equation for R_G becomes,

$$R_G = \frac{50\ \text{k}\Omega}{A_v - 1}$$

If R_G is left as infinity, the voltage gain is 1, while $R_G = 50\ \Omega$ give a voltage g
approximately 1000. Resistor R_6 is trimmed by the manufacturer to yield a co
mode rejection ratio greater than 80 dB. R_6 is also terminated at pin 9, which i
ally grounded. Instead of grounding pin 9, it can be connected to a bias v
source for dc output voltage level control. The LH0036 has an input impedan

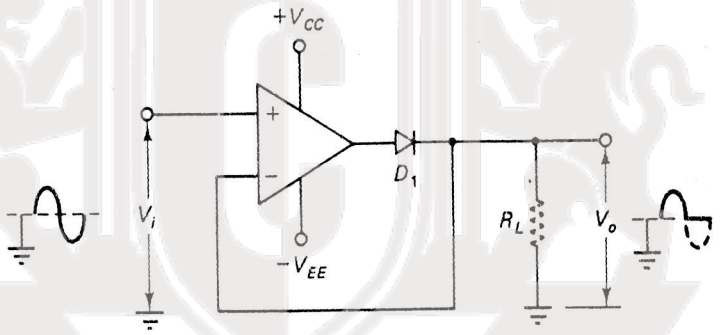
INTRODUCTION

The use of operational amplifiers can improve the performance of a wide variety of signal processing circuits. In rectifier circuits, the voltage drop that occurs with an ordinary semiconductor rectifier can be eliminated to give precision rectification. Waveforms can be limited and clamped at precise levels when op-amps are employed in clipping and clamping circuits. The errors that occur with peak detectors and sample-and-hold circuits can also be minimized by the use of op-amps.

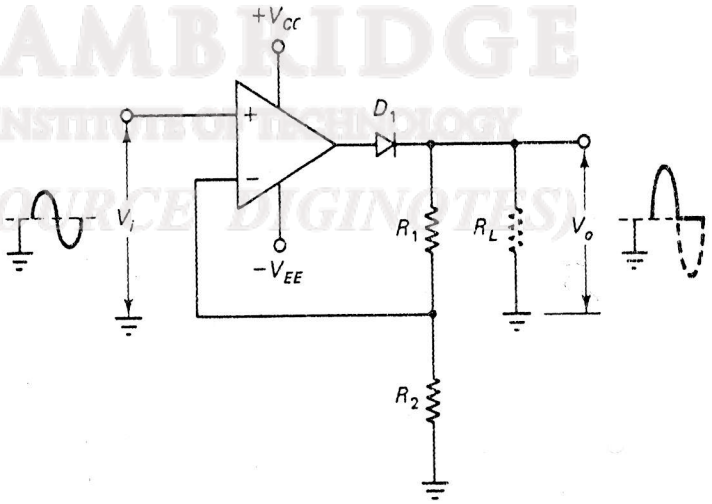
7-1 PRECISION HALF-WAVE RECTIFIERS

Saturating Precision Rectifier

The circuit of an op-amp *precision half-wave rectifier*, illustrated in Fig. 7-1(a), is simply a voltage follower with a diode inserted between the op-amp output terminal and the circuit output point. When the input signal is positive, the diode is forward



(a) Saturating precision half-wave rectifier circuit



(b) Saturating precision half-wave rectifier with voltage gain

Figure 7-1 Including a diode at the output of a voltage follower or a noninverting amplifier converts the circuit into a precision half-wave rectifier. Because the op-amp output saturates when the diode is reversed, there is a relatively long recovery time.

biased and the output voltage follows the input. Recall that negative feedback causes the voltage at the inverting input terminal to follow that at the noninverting terminal. Since the output of the circuit and the inverting terminal are common, the output follows the input within microvolts. The diode forward voltage drop is not involved.

While the input voltage is in its negative half-cycle the op-amp output is negative and the diode is reverse biased. Consequently, the feedback path is interrupted, the inverting input terminal remains at ground level (because R_L is grounded), and the op-amp output is saturated in a negative direction. The negative half-cycle of the input does not pass to the output; it is clipped off. If the diode polarity is reversed in Fig. 7-1(a), the negative half-cycle of the input waveform will be passed to the output and the positive half-cycle will be clipped off.

The advantages of the op-amp precision rectifier circuit over a simple diode rectifier are (1) no diode voltage drop between input and output, (2) the ability to rectify very small voltages (less than the typical 0.7 V diode forward voltage drop), (3) amplification, if required, and (4) low output impedance. Items (1) and (2) indicate that the precision rectifier is a close approximation to an ideal diode.

While the input waveform is in its negative half-cycle, the output of the op-amp in Fig. 7-1(a) is saturated in a negative direction. Some time is required to get the op-amp out of saturation and this will limit the frequency response of the circuit. For high frequency performance, a nonsaturating precision rectifier circuit must be used.

Figure 7-1(b) shows the circuit of a precision rectifier with voltage gain. This is a noninverting amplifier with the diode included. The circuit is designed exactly as a noninverting amplifier, except that the current through R_1 and R_2 should be a minimum of about 100 μA to ensure that the diode is operating correctly in the absence of a load current. A minimum diode current of 500 μA is a good design objective.

Nonsaturating Precision Rectifier

The precision rectifier circuit in Fig. 7-2 uses an inverting amplifier configuration. Diode D_1 is reverse biased and D_2 is forward biased when the op-amp output terminal is positive. This occurs when the input signal is negative. While D_2 is forward biased, the circuit output is

$$V_o = -V_i \frac{R_2}{R_1}$$

If R_2 equals R_1, V_o equals $-V_i$ during the negative half-cycle of the input. If R_2 is greater than R_1, the output is an amplified (inverted and half-wave rectified) version of the input.

During the positive half-cycle of the input, the op-amp output terminal goes negative, causing D_2 to be reverse biased. Without D_1 in the circuit, the op-amp output would be saturated in a negative direction. However, the negative voltage at the op-amp output forward biases D_1. This tends to pull the op-amp inverting input ter-

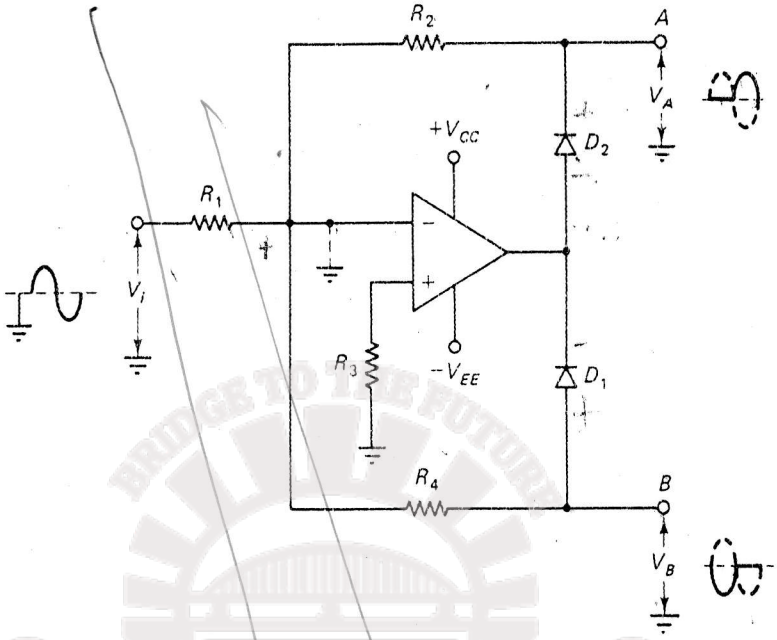


Figure 7-3 Two-output precision half-wave rectifier. D_1 is forward biased during the positive half-cycle, D_2 during the negative half-cycle. In each case, the circuit behaves as an inverting amplifier.

with the op-amp to perform as an inverting amplifier. The output at terminal A is

$$V_A = -(-V_i)\frac{R_2}{R_1}$$

With D_1 reversed, no current flows in resistor R_4; and with R_4 connected to the virtual ground at the op-amp inverting input, the output at terminal B is zero.

The circuit in Fig. 7-3 is seen to be a precision rectifier with positive half-cycles of output at terminal A, and negative half-cycles at terminal B.

7-2 PRECISION FULL-WAVE RECTIFIERS

Half-Wave Rectifier and Summing Circuit

The left side of the circuit in Fig. 7-4 is a precision half wave rectifier as in Fig. 7-2 but with the diodes reversed. The right side is an inverting summing amplifier circuit, (explained in Section 3-5). The input voltage is applied to terminal A of the summing amplifier and to the input of the precision rectifier. Note that resistor R_2 in the precision half-wave rectifier circuit has twice the resistance of R_1, so the rectified voltage applied to terminal B of the summing amplifier is $-2\ V_i$, as illustrated.

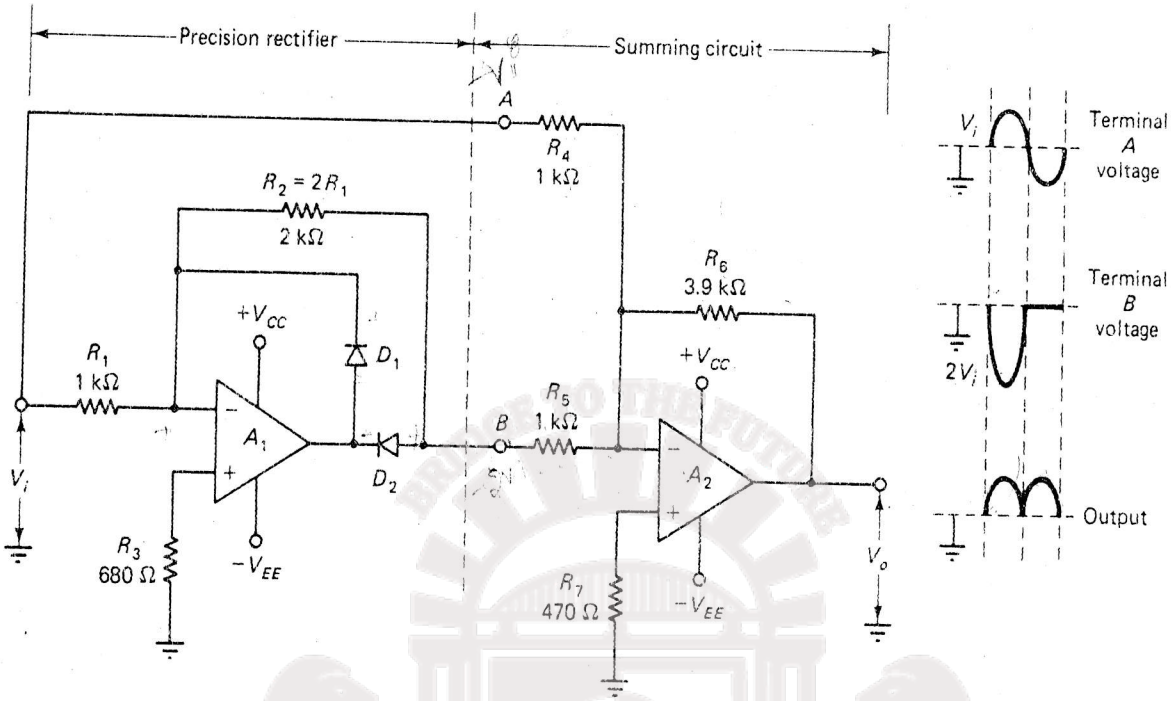


Figure 7-4 Full-wave precision rectifier consisting of a summing circuit and a precision half-wave rectifier which has a voltage gain of 2. During the input positive half-cycle, $-2V_i$ is summed with V_i and the result is inverted. During the negative half-cycle, V_i and zero are summed and inverted.

During the positive half-cycle of the input, the voltage at terminal A is $+V_i$, while that at terminal B is $-2\,V_i$. The output from the summing circuit with $R_5 = R_4$ is

$$V_o = -\frac{R_6}{R_4}(V_A + V_B)$$

$$= -\frac{R_6}{R_4}(V_i - 2\,V_i)$$

$$= \frac{R_6}{R_4}V_i$$

During the negative half-cycle of the input, $V_A = -V_i$, and $V_B = 0$. Consequently, the output is

$$V_o = -\frac{R_6}{R_4}(-V_i + o)$$

$$= \frac{R_6}{R_4}V_i$$

It is seen that the output is a full-wave rectified version of the input voltage. If resistor R_6 equals R_4 and R_5, the circuit has an overall voltage gain of 1. When R_6 is

greater than R_4 and R_5, amplification and rectification both occur. A precision full-wave rectifier circuit is also known as an *absolute value circuit*. This means the circuit output is the absolute value of the input peak voltage regardless of the input polarity.

Example 7-2

Design a precision full-wave rectifier circuit as in Fig. 7-4, to produce a 2 V peak output from a sine wave input with a peak value of 0.5 V and a frequency of 1 MHz. Use bipolar op-amps with a supply voltage of ±15 V.

Solution

$$I_1 \gg I_{B(\max)}$$

let $I_1 = 500\ \mu\text{A}$ (for adequate diode current)

$$R_1 = \frac{V_i}{I_1} = \frac{0.5\ \text{V}}{500\ \mu\text{A}}$$

$$= 1\ \text{k}\Omega \quad \text{(standard value)}$$

$$R_2 = 2\,R_1 = 2\ \text{k}\Omega \quad \text{(use two 1 k}\Omega\text{ resistors in series)}$$

$$R_3 = R_1 \parallel R_2 = 1\ \text{k}\Omega \parallel 2\ \text{k}\Omega$$

$$= 670\ \Omega \quad \text{(use 680 }\Omega\text{ standard value)}$$

$$R_4 = R_5 = R_1 = 1\ \text{k}\Omega \quad \text{(standard value)}$$

For the output to be 2 V when the input is 0.5 V,

$$R_6 = \frac{V_o}{V_i} \times R_5 = \frac{2\ \text{V}}{0.5\ \text{V}} \times 1\ \text{k}\Omega$$

$$= 4\ \text{k}\Omega \quad \text{(use 3.9 k}\Omega\text{ standard value)}$$

$$R_7 = R_4 \parallel R_5 \parallel R_6 = 1\ \text{k}\Omega \parallel 1\ \text{k}\Omega \parallel 3.9\ \text{k}\Omega$$

$$= 443\ \Omega \quad \text{(use 470 }\Omega\text{ standard value)}$$

For diodes D_1 and D_2, $V_R > 30$ V, and $t_{rr(\max)} = 0.1\ \mu$s as in Example 7-1.

Compensate A_1 as a voltage follower, and A_2 for a gain of

$$\frac{R_6 + R_4 \| R_5}{R_4 \| R_5} \simeq 9$$

opposition offered by resistance to flow of current

High Input Impedance Full-Wave Precision Rectifier

A precision rectifier that uses a noninverting amplifier configuration to present a high input impedance to the signal is shown in Fig. 7-5. Op-amp A_1 together with resistors R_3 and R_4 constitutes a noninverting amplifier, as does A_2, R_5 and R_6. However, diodes D_1 and D_2 also affect the operation of the circuit.

Consider what occurs during the positive half-cycle of the input waveform. The output terminal of A_2 is positive, D_2 is forward-biased, and D_1 is reversed. The

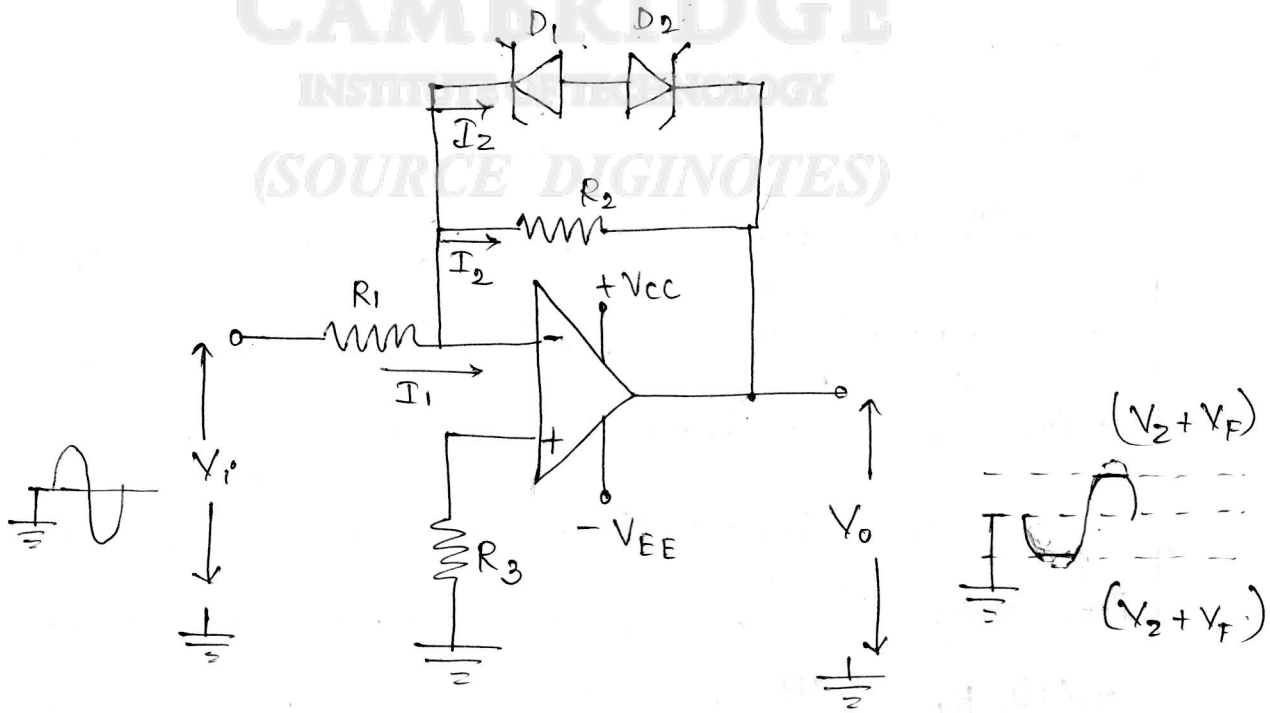
Module 3

Applications of opamp.

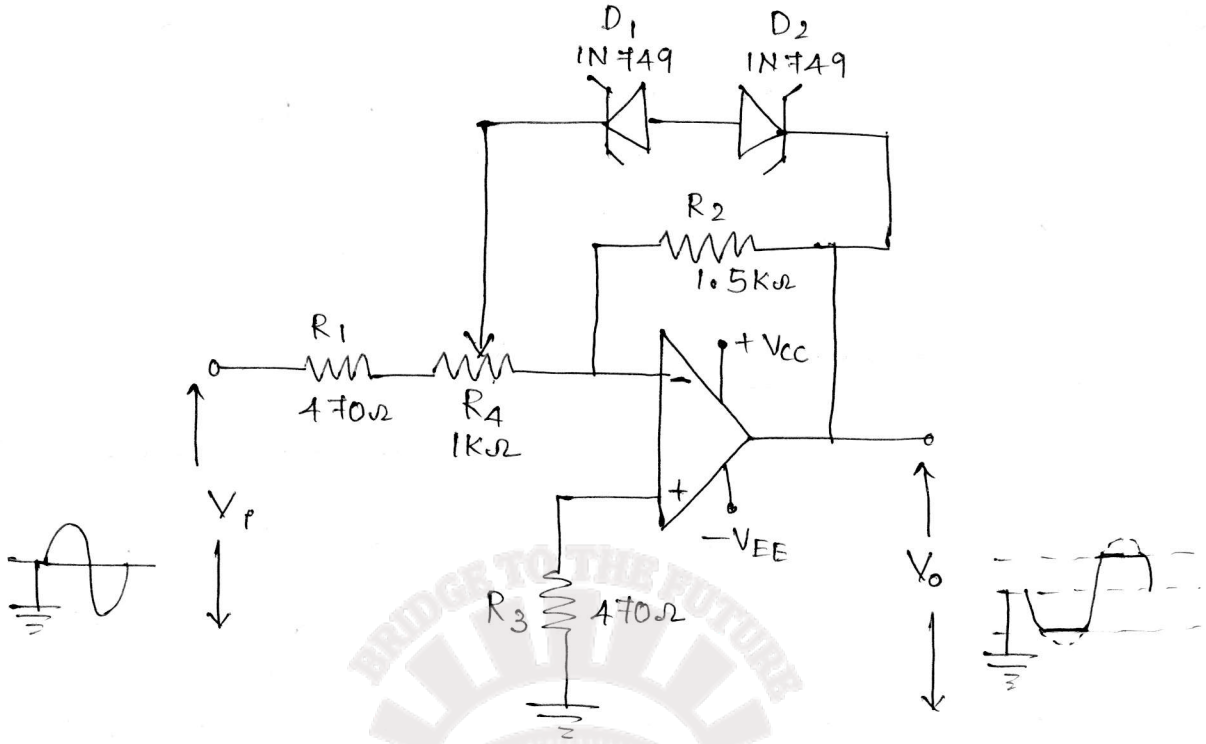
Limiting circuits

Peak clipper

Back to back connected zener diodes are used in the circuit of fig (a) to clip off the peaks of the output voltage waveform. One diode is forward biased and the other is biased into reverse breakdown when the output voltage is greater than $(V_F + V_Z)$; that is the forward voltage drop of one diode plus the zener break down voltage of the other.



(a) Zener diode peak clipper.



(b) Adjustable peak clipper.

Negative feedback causes the opamp output to remain at the level that keeps the inverting input terminal close to the voltage at the (grounded) non-inverting input. Thus, as illustrated, the output cannot exceed $\pm(V_F + V_Z)$. As long as the output voltage is less than this limit, the circuit behaves as an inverting amplifier amplifier unaffected by the diodes. This kind of circuit is typically used to protect a device that might be damaged by excessive input voltage.

Figure (b) shows a circuit modification in which variable resistor R_4 is connected in series with R_1. With the zener diodes connected to the

moving contact of R_4, as illustrated, the output limiting voltage can be adjusted. Suppose that $R_1 = R_4 = R_2$ and that $(V_Z + V_F) = 4V$. With the moving contact at the right side of R_4

$$V_{o(max)} = V_Z + V_F = \pm 4V$$

With the moving contact at the left side of R_4

$$V_{R_2} + V_{R_4} = V_Z + V_F = \pm 4V$$

and with $R_2 = R_4$

$$V_{R_2} = V_{R_4} = \pm 2V$$

giving $V_{o(max)} = V_{R_2} = \pm 2V$

By means of the moving contact, the maximum output voltage can be adjusted between $\pm 2V$ and $\pm 4V$. To design a peak clipper, the zener diodes are first selected to limit the output voltage at the desired level, bearing in mind that V_F is typically 0.7 V. The resistor current must be greater than the minimum level required for zener breakdown, typically around 0.5mA.

Problem.

1) Design an adjustable peak clipping circuit to clip at approximately ± (3V to 5V). The circuit is to have unity voltage gain before clipping

$\longrightarrow$ $V_{o(max)} = V_Z + V_F \simeq 5V$

$V_Z = 5V - V_F \simeq 5V - 0.7V$

$\simeq 4.3V$ (use a 1N 749 zener diode)

$I_1 > (I_{Z(min)} = 500\mu A)$

Let $I_{1(min)} = 2mA$.

For $V_o \simeq 3V$

$R_2 = \frac{V_{o(min)}}{I_{1(min)}} = \frac{3V}{2mA} = 1.5k\Omega$ (standard value)

$V_{R4} = V_{o(max)} - V_{o(min)} = 5V - 3V$

$= 2V$

$R_4 = \frac{V_{R4}}{I_1} = \frac{2V}{2mA}$

$= 1k\Omega$ (standard potentiometer value)

For $A_c = 1$, $R_1 + R_4 = R_2$

or, $R_1 = R_2 - R_4 = 1.5k\Omega - 1k\Omega$

$= 500\Omega$ (use 470Ω standard value)

$R_3 = (R_1 + R_4) \| R_2$

$= (470\Omega + 1k\Omega) \| 1.5k\Omega$

$R_3 = 742\Omega$ (use 680Ω standard value)

Dead zone circuit

The circuit in fig (a) is a precision half wave rectifier with the addition of resistor R_1 and dc reference voltage V_{ref}. If R_1 and V_{ref} were absent, the circuit would simply produce an inverted half wave rectified version of the input. Note that if the diodes were absent (D_1 open circuited and D_2 short circuited), the arrangement would constitute an inverting summing circuit. When the opamp output goes positive, forward biasing D_2 and reversing D_1, the circuit functions exactly as a summing circuit, giving an output of

$$V_o = -(V_{ref} + V_i)$$

V_{ref} is a positive quantity. If V_i equals zero, V_{ref} tends to drive the opamp output in a negative direction. In this situation D_1 becomes forward-biased and V_o remains at ground level. To drive the opamp output output terminal in a positive direction, V_i must be negative and have a level greater than the positive level of V_{ref}.

$$|-V_i| = |+V_{ref}|$$

When this occurs, D_2 is forward biased, D_1 is reversed, and as already stated, the output becomes the sum of V_{ref} and V_i. Suppose V_{ref} is +1 and V_i is −4 V

$$V_0 = -(V_{ref} + V_i) = -[1V + (-4V)]$$

$$V_0 = 3V.$$

The circuit output remains at ground level until $|-V_i|$ exceeds $|+V_{ref}|$. Then the output is the peak portion of the (negative) input that exceeds the reference voltage level. Only this part of the input wave is passed (and inverted). All other portions of the input wave are ineffective. The ineffective portions of the input are said to occupy a dead zone.

Problem

1) Using BIFET opamp, design a dead zone circuit to pass only the upper 1V portion of the positive half cycle of a sine wave input with a peak value of 3V.

Circuit diagram for dead zone circuit

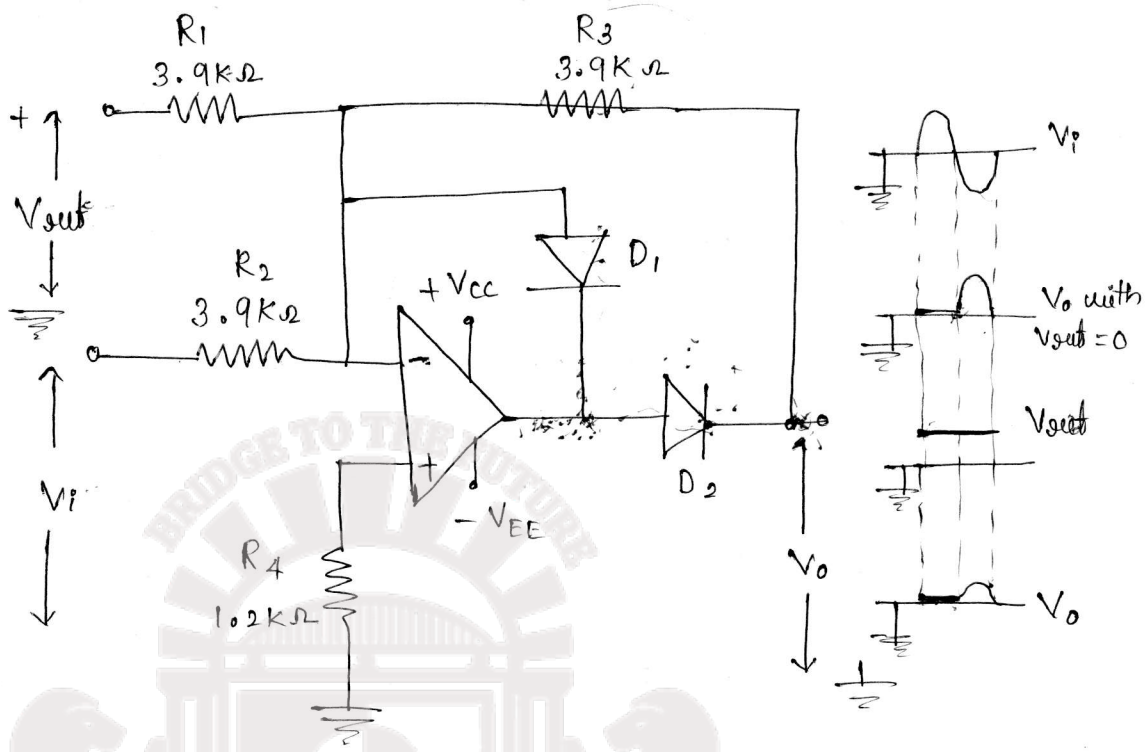


fig (a)

Problem

1) Using BIFET opamp, design a dead zone circuit to pass only the upper 1V portion of the positive half cycle of a sine wave input with a peak value of 3V.

→ $V_{out} = V_p - 1V = 3V - 1V$

$= 2V$

$I_{R1}(min) = I_D(min) = 500\mu A$

$R_1 = \frac{V_{out}}{I_{R1}} = \frac{2V}{500\mu A}$

$= 4K\Omega$ (use $3.9K\Omega$ standard value)

$R_2 = R_3 = R_1 = 3.9K\Omega$

$R_4 = R_1 || R_2 || R_3 = 3.9K\Omega || 3.9K\Omega || 3.9K\Omega$

$= 1.3K\Omega$ (use $1.2K\Omega$ standard value)

Clamping circuits

Diode clamping circuit:

A clamping circuit reproduces an input waveform without any clipping or distortion, but limits the upper or lower peak of the waveform to a predetermined level.

Consider the diode clamping circuit in (a). When the i/p vtg is positive, diode D_1 is forward biased and capacitor C_1 charges with the polarity shown. The peak input voltage (V_p) appears across C_1 and D_1 so the capacitor charges to

$$V_{C_1} = V_p - V_F$$

At this time, the output voltage cannot exceed the voltage drop across the forward biased diode.

$$V_o = V_F$$

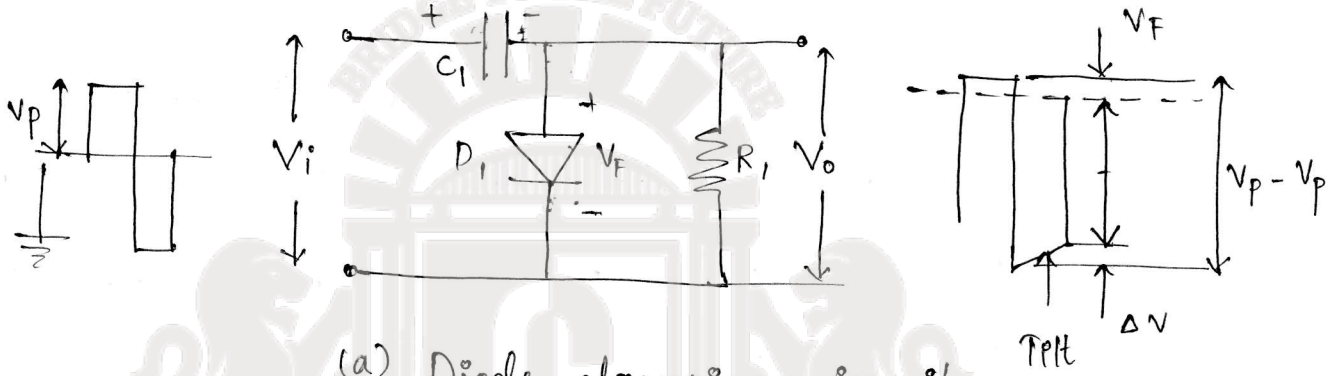
When the input goes to its negative peak, D_1 is reverse biased and the input and capacitor voltages combine to produce an output of

$$V_0 = -V_p - V_{C1}$$
$$= -V_p - (V_p - V_F)$$
$$= -2V_p + V_F$$

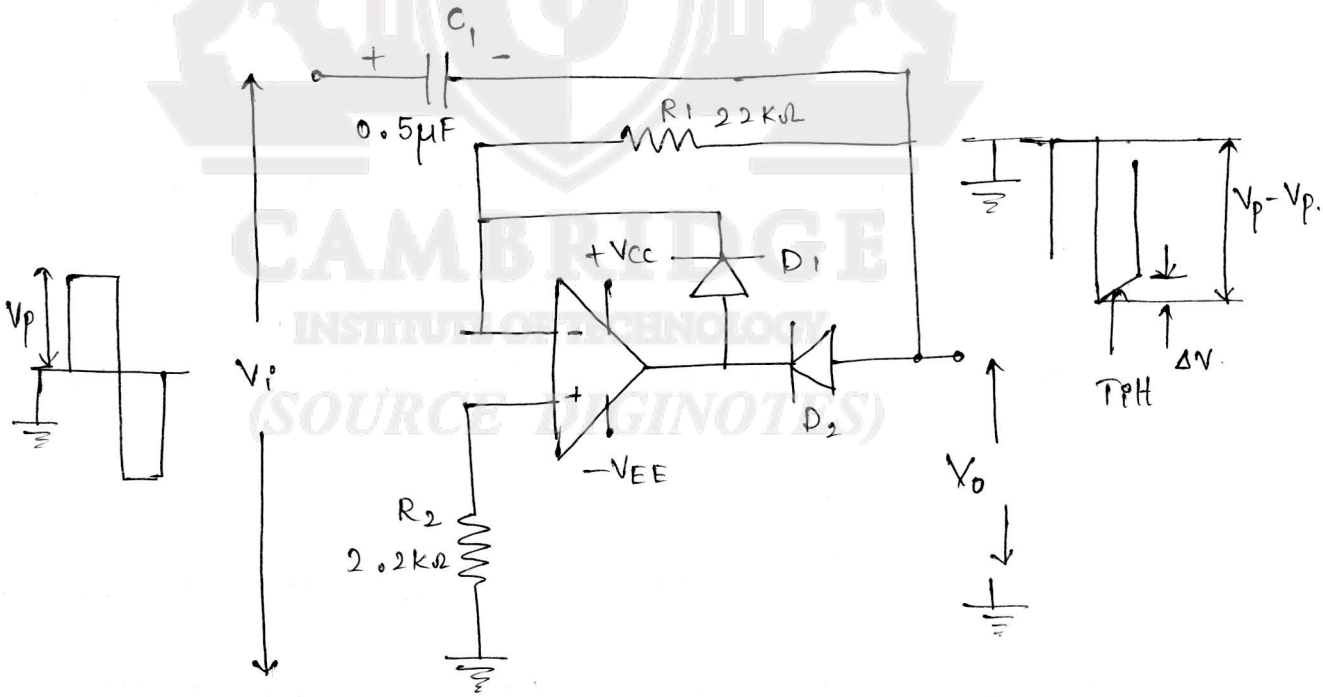
As illustrated, the output waveform has the same peak to peak amplitude as the ~~output's~~ input, but its upper level is clamped at V_F. If the diode is reversed, the lower level of the output would be clamped at $-V_F$. In this case, the capacitor polarity should also be reversed. A bias voltage (V_B) could be connected in series with the diode and ground to give a clamped output level of $+(V_B + V_F)$ or $(-V_B + V_F)$.

The function of resistor R_1 in fig (a) is to ensure the capacitor discharges when the peak input voltage drops to a lower level. R_1 produces tilt (or slope) on the unclamped peak of the output, as illustrated.

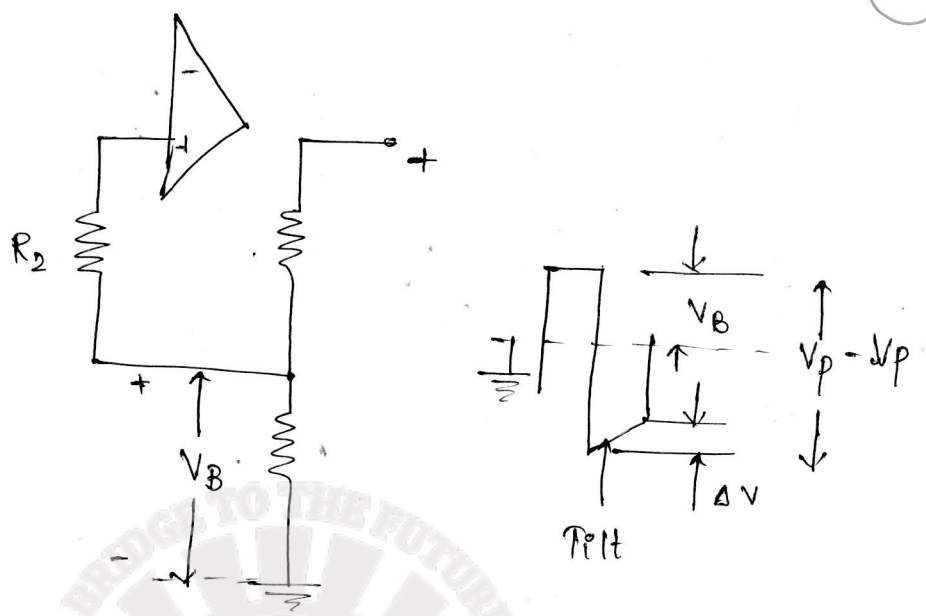
This can be minimized by keeping R_1 as large as possible. Any load resister at the circuit output will be in parallel with R_1 and will increase the tilt on the output wave form.



(a) Diode clamping circuit.



(b) Precision clamping circuit.



Peak detectors

Voltage follower peak detector

In the peak detector circuit (a) the only capacitor discharge currents are the input bias current to op-amp. A_2 and the reverse leakage current of diode D_2. Because op-amp A_1 is connected as a voltage follower, the circuit presents a very high input impedence to the signal source. Opamp A_2 is also connected to function as a voltage follower, so output V_o always equals capacitor voltage V_C. With resistor R_2 connected from the circuit output to the inverting input terminal of A_1, V_C also apears at that terminal.

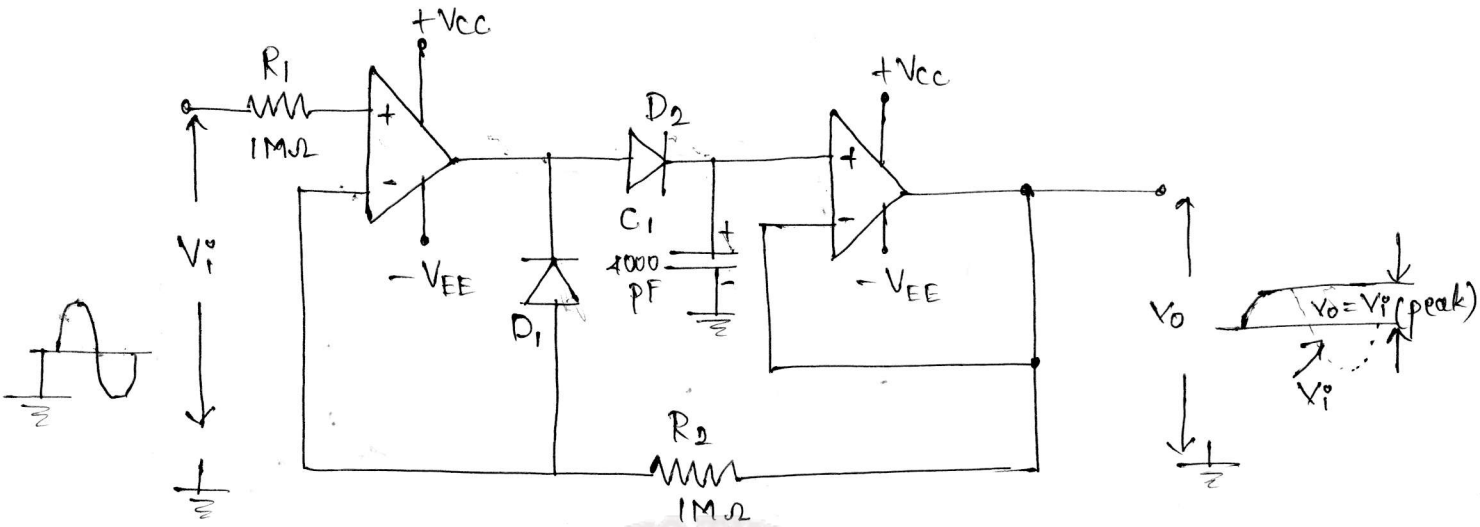


fig ⓐ.

When V_i is greater than V_c, the output of A_1 is positive, D_2 is forward-biased, and A_1 behaves as a voltage follower, charging C_1 to V_p. When V_i falls below V_p, V_c remains at V_p, and consequently, the inverting input terminal of A_1 also remains at V_p. Therefore, the output of op-amp A_1 goes negative, reversing D_2 and forward biasing D_1. Negative feedback via D_1 keeps A_1 from going into saturation.

In the circuit fig ⓐ. A_2 should be a BIFET op-amp for low input bias current, but A_1, can be any op-amp type that is otherwise suitable. Once again, diode D_2 should have a very low reverse leakage current. However, with the use of a BIFET op-amp for A_2, the reverse leakage of D_2

is likely to be much larger than the input bias current of A_2, Therefore, the diode reverse leakage current $I_{R(D2)}$ is more effective in discharging C_1 than $I_{B(max)}$ of A_2. Capacitor size and opamp slew rate calculated as already discussed, and C_1 should have a very high resistance dielectric

Problem

1) A peak detector circuit as in fig ⓐ. is to be designed. The pulse-type signal voltage has a peak value of approximately 2.5 V with a rise time of 5 μs, and the output voltage is to be held at 2.5 V for a time of 100 μs. The maximum output error is to be approximately 1%. Calculate the required component values and specify the output current and slew rate of the operational amplifier.

→ Use BIFET op-amp for minimum capacitor leakage current.

Let $R_1 = R_2 = 1M\Omega$

C_1 discharge current, $I_d = I_{R(D2)} \simeq 1\mu A$.

$\Delta V = 1\%$ of $V_p = 1\%$ of $2.5\,V$

$= 25\,mV$.

$$C_1 = \frac{I_d t_h}{\Delta V} = \frac{1\mu A \times 100\mu s.}{25mV}$$

$$= 4000\,pF \quad \text{(standard value)}$$

For opamp A_1,

$$I_{o(max)} = \frac{C_1 V_p}{t_r} = \frac{4000pF \times 2.5V}{5\mu s.}$$

$$= 2mA.$$

$$\text{Min slew rate} \simeq 3\frac{V_p}{t_r} = \frac{3 \times 2.5\,V}{5\mu s.}$$

$$= 1.5\,V/\mu s.$$

* Sample and Hold Circuits

Op-amp sample and Hold

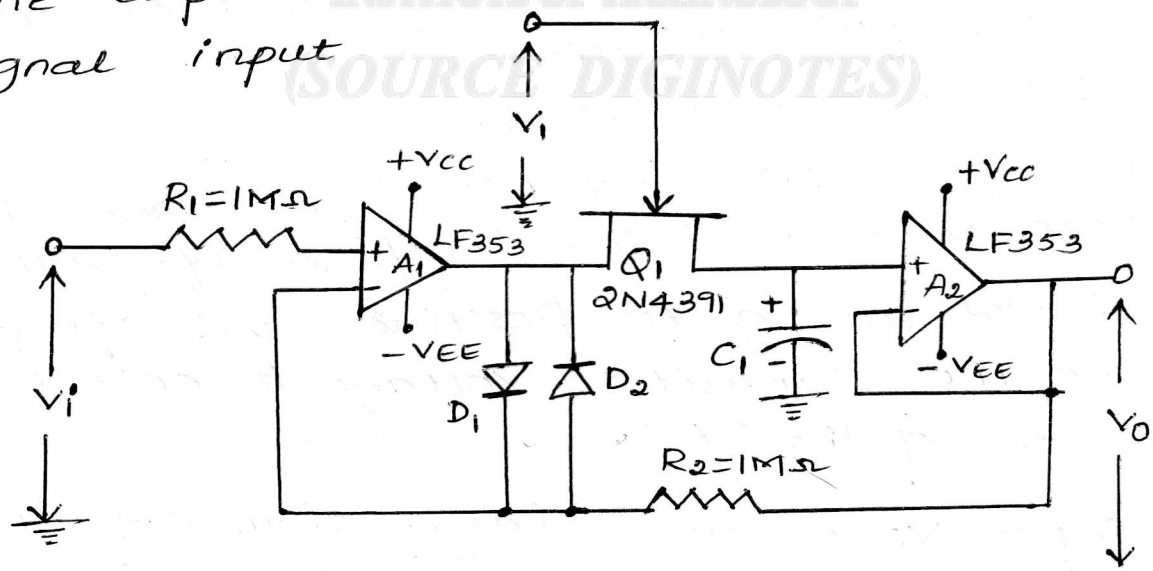
A sample and hold circuit samples instantaneous amplitudes of a signal voltage at any point in its waveform and holds the voltage level constant until the next sample is acquired

fig (a) is the modified version of peak detector circuit 1) The Modifications are that FET switch Q_1 is included to alternately connect and disconnect the capacitor at the output of op amp A_1.

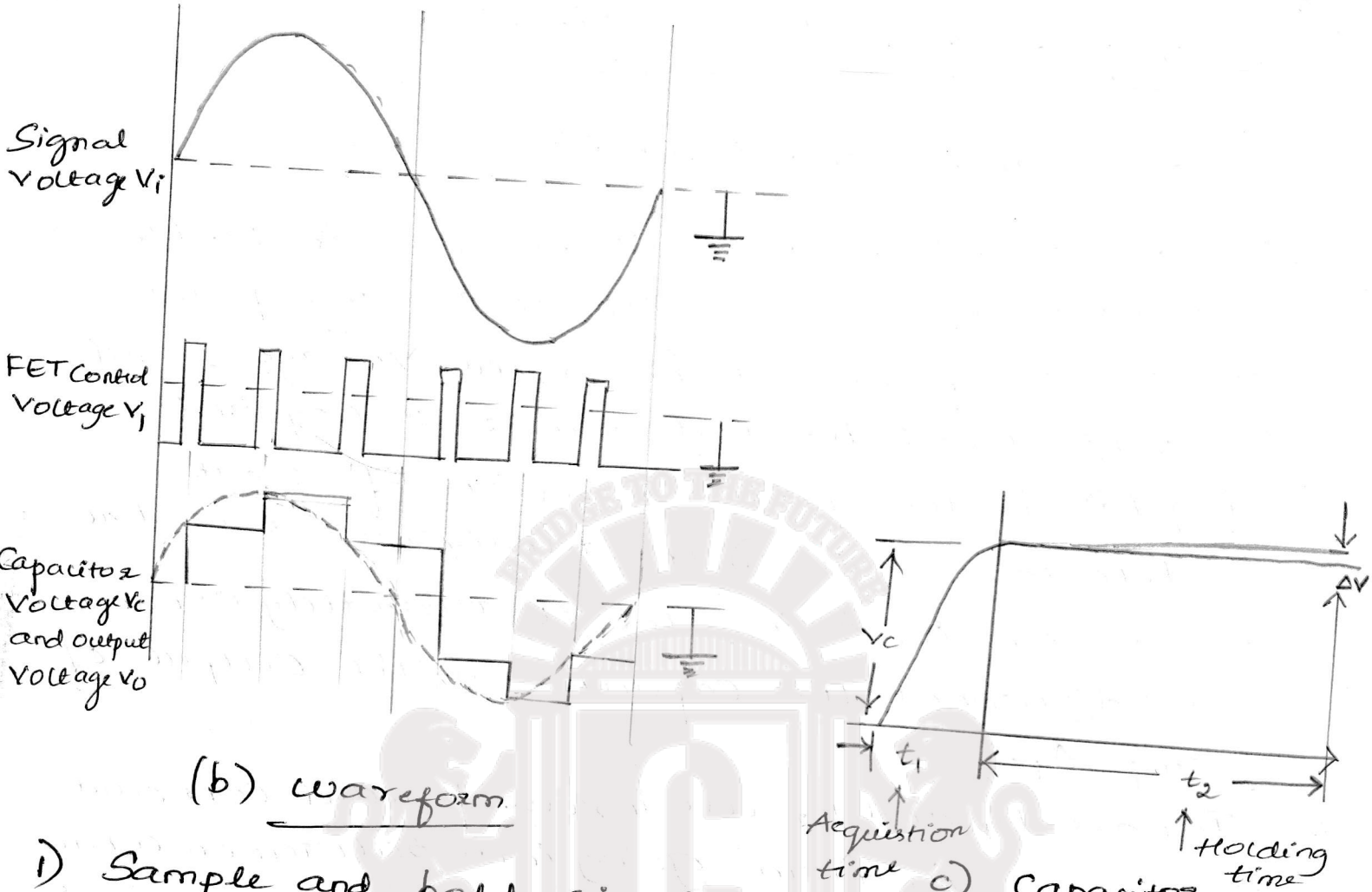
2] Diodes D_1 and D_2 are inverse parallel connected to prevent A_1 from going into saturation when Q_1 is open-circuited.

3] with Q_1 switched on, A_1 and A_2 act as a single voltage follower, exactly as in the circuit of fig (a).

4) The capacitor voltage precisely follows the signal input



(a) Sample and hold circuit.



(b) waveform

c) Capacitor Voltage

1) Sample and hold circuit which functions similarly to the voltage follower type peak detector but with the addition of switching FET Q_1 to periodically switch V_i to C_1

2) The waveforms in fig (b) illustrate the circuit operation. Q_1 is repeatedly switched on and off by the pulse waveform (control voltage V_1) applied to its gate terminal.

3) V_1 must go sufficiently negative to drive the FET gate voltage below its pinch-off voltage

4) It should also go to positive level approximately equal to the capacitor voltage to ensure complete turn on of the FET.

5) If input V_i becomes larger than capacitor voltage V_c while Q_1 is off, C_1 rapidly charges to the level of V_i when Q_1 switches ON.

6] When Q_1 is off, only the input bias current to A_2 and the FET gate source reverse leakage current are effective in discharging the capacitor so, C_1 holds the sampled voltage constant until the next sampling instant, giving the step type capacitor voltage (and output) illustrated in fig(b).

7) During the sampling time, or acquisition time (t_1 in fig (c)], C_1 is charged via the FET channel resistance $R_{D(on)}$. If the sampling time is

$$t_1 = 5 C R_{D(on)} \rightarrow (1)$$

8) The capacitor is charged to 0.993 of the input voltage, resulting in a 0.7% error in the sample amplitude

$$t_1 = 7 C R_{D(ON)} \rightarrow (2)$$

9) If $t_1 = 7 C R_{D(ON)}$ is used, the error is 0.1%. During the holding time (t_2 in fig(c)), the capacitor is partially discharged, exactly like peak detector circuit.

10] So, $C_1 = \frac{I_d t_h}{\Delta V}$ can be used to calculate capacitor value and eqn (1) or (2) can be employed to determine the minimum acquistion time.

Op-amp A_2 should have a very low input bias current, Q_1 should have a very low gate-source leakage current, and the capacitor should have a low leakage dielectric. Q_1 should also have a low channel resistance for rapid charge and discharge C_1. The FET gate-source capacitance (C_{GS}) can be one more source of error. C_{GS} charges when the FET

is switched off and this charge is removed from Capacitor C_1.

* Problem Regarding Sample and hold Ckt.

1) A Sample and hold circuit as shown in fig(a) has a signal amplitude of 1V which is to be sampled with an accuracy of approximately 0.2%. The holding time is to be 500μs. Design the circuit using LF353 BIFET op-amps and a 2N4391 FET. Determine the minimum acquistion time.

Soln:- For the LF353 op-amp

$$I_{B(max)} = 50pA$$

For the 2N4391 FET, the gate source reverse Current is

$$I_{GS} = 200nA$$

and the channel resistance when ON is

$$R_{D(ON)} = 30\Omega$$

let $R_1 = R_2 = 1M\Omega$

Capacitor discharge current

$$I_d \simeq I_{GS} \simeq 200nA$$

For a 0.2% total error, allow 0.1% due to capacitor discharge and a 0.1% charging error

For 0.1% error due to discharge during the holding time.

let $\Delta V = 0.1\%$ of $V_i = 0.1\%$ of 1V

$$= 1mV$$

⑤ (10)

$$C_1 = \frac{I_d t_h}{\Delta V} = \frac{200nA \times 500\mu s}{1mV}$$

$$= 0.1\mu F \quad (\text{Standard value})$$

For the 2N 4391, $V_{GS(OFF)} = 10V$ maximum

Therefore $V_1(-) = -10V$

$V_1(+) \simeq V_o$

$= +1V$

for 0.1% error due to acquistion time,

$$t_i(min) = 7CR_{D(ON)}$$

$$= 7 \times 0.1\mu F \times 30\Omega$$

$$= 21\mu s.$$

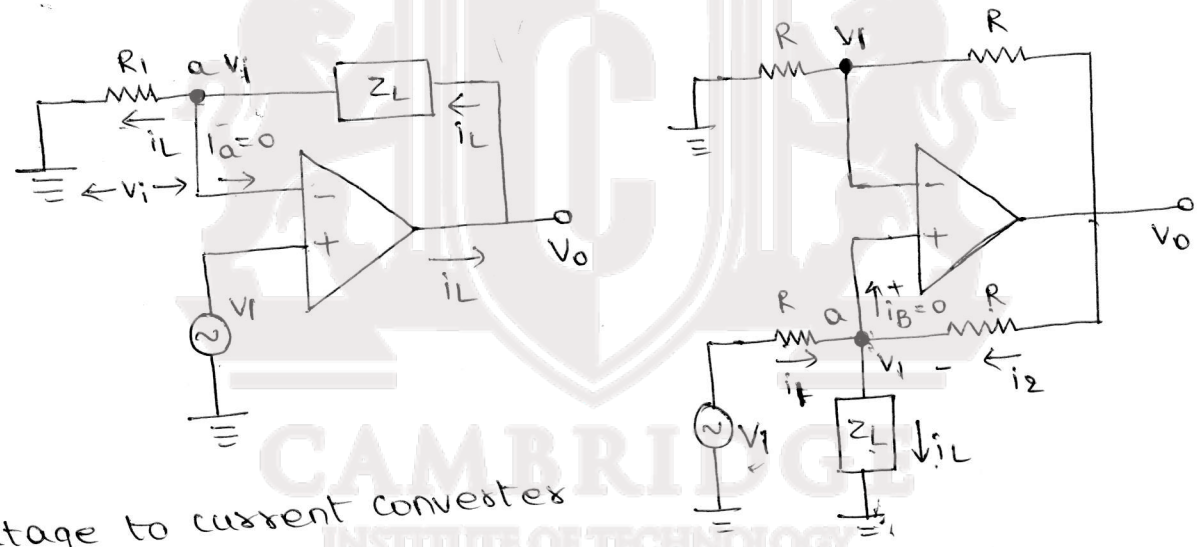
V TO I AND I TO V CONVERTER

Voltage to current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuit possible.

V-I converter with floating load

V-I Converter with grounded load



Voltage to current converter with

a) Floating load

b) Grounded load

The above fig a) shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is V_i, therefore

$$V_i = i_L R_1 \qquad (\text{as } I_B = 0)$$

(or), $$i_L = \frac{V_i}{R_1}$$

That is the Input voltage V_i, converted into an output current of V_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore signal source should be capable of providing this load current.

A voltage-to-current converter with grounded load is shown in fig b). Let V_1 be the voltage at node 'a'. writing KVL, we get

$$i_1 + i_2 = i_L$$

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o - 2V_1 = i_L R$$

Therefore,

$$V_1 = \frac{V_i + V_o - i_L R}{2}$$

Since the op-amp is used in non-Investing mode, the gain of the circuit is $1 + \frac{R}{R} = 1 + 1 = 2$. The output voltage is,

$$V_o = 2V_1 = V_i + V_o - i_L R$$

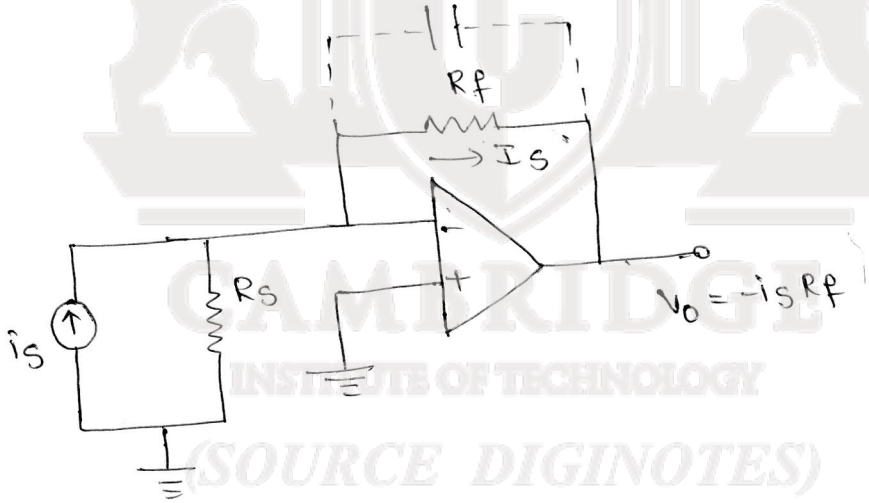
$$V_i = i_L R$$

$$i_L = \frac{V_i}{R}$$

As the Input Impedance of a non-Investing ampli. is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

Current to voltage Converter (Transresistance Amplifier)

Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo device can be measured.



The above figure, shows an op-amp used to I to V converter. Since the (−) Input terminal is at virtual ground, no current flows through Rs and current is flows through the feedback resistor Rf. Thus the output voltage $V_o = -i_s R_f$

It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the op-amp.

This means that μA741 (I_B =) can be used to detect lower currents. The resistor Rf is sometimes shunted with a capacitor Cf to reduce high frequency noise and the possibility of oscillations.

⇒ Differentiating Circuit:-

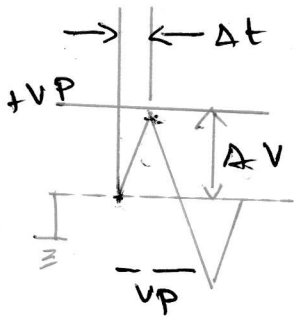
(*) A differentiating circuit produces an output voltage which is proportional to the rate of change of the input voltage. Differentiation can be performed by a simple RC series circuit in which the output is taken as the voltage across resistor.

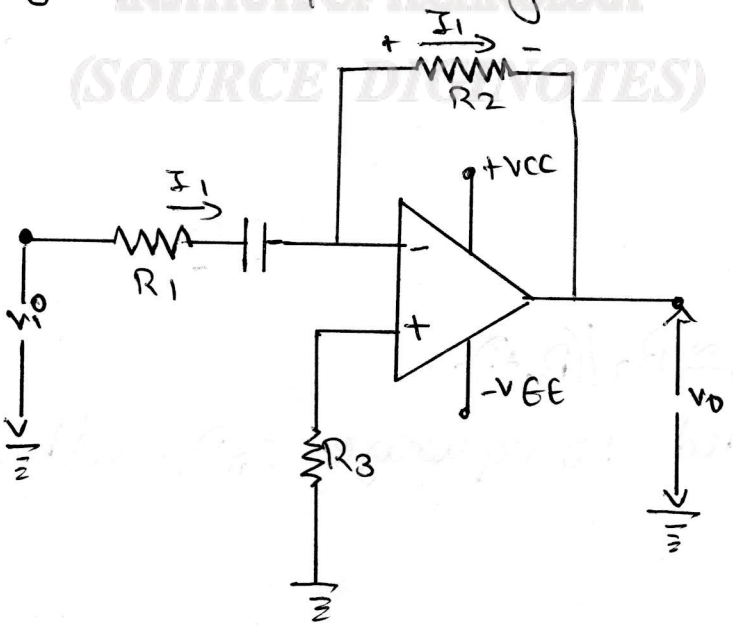
(*) However the OP-AMP differentiating circuit has a much lower output resistance and higher output voltage than is possible with a simple RC circuit.

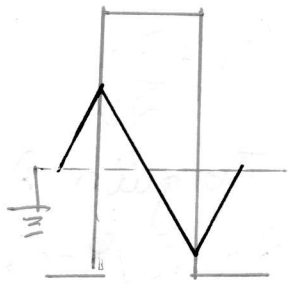
(*) The circuit behaves as a voltage follower with the non-inverting input grounded

(*) When the input signal is a positive going voltage, a current I_1 flows into C_1, as illustrated with I_1 much larger than the maximum input bias current to the OP-AMP effectively all of I_1 flows through R_2.

(*) The left side of R_2 at the OPAMP inverting input remains close to ground and, as for an inverting amplifier, the output voltage is $V_0 = -I_1 R_2$







$V_0 = -C_1 R_1 \frac{\Delta v}{\Delta t}$

Consider the case of the triangular waveform illustrated, when positive going, it has a rate of change easily identified as $\Delta V/\Delta t$.

∴ With a constant charging current

$$C_1 = \frac{I_1 \Delta t}{\Delta V}$$

$$I_1 = \frac{C_1 \Delta V}{\Delta t}$$

$$\therefore \quad V_0 = -\frac{C_1 \Delta V}{\Delta t} \times R_2 \;/\; -C_1 R_2 \frac{\Delta V}{\Delta t}$$

(*) This is the output voltage which is directly proportional to the rate of change of the input, or the output is the derivative of the input, because of differentiated output of the circuit is inverted.

(*) Resistor R_1 in series with capacitor C_1 is included to help prevent the circuit from oscillating at high frequencies.

(*) The inclusion of R_1 corrects the phase lag and usually allows the circuit to be compensated for a closed loop gain of R_2/R_1. R_1 also has some effect on the circuit performance as a differentiator.

Design:-

$$R_2 = \frac{V_0}{I_1}$$

$$R_1 = \frac{R_2}{20}.$$

∴ The gain $A_0 \simeq R_2/(R_1+R_3)$

R_3 is included to equalize $I_B R_B$ voltage drop

∴ $R_3 = R_2$.

Problem:-

Design a differentiating circuit to give an output of 5V when the input changes by 1V in a time of 100μs. Use an OPAMP with a bipolar input stage.

Sol

$I_1 >> I_{B\,max}$

$I_1 = 500\mu A$.

$R_2 = \frac{V_0}{I_1} = \frac{5V}{500\mu A} = 10k\Omega$. (Standard value)

$C_1 = \frac{I_1 \times \Delta t}{\Delta_0} = \frac{500\mu A \times 100\mu s}{1V} = 0.05\mu f$. (Standard value)

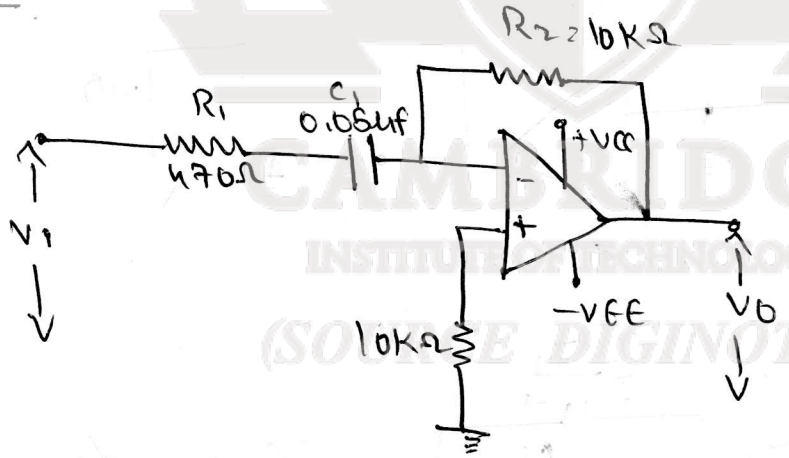
$R_1 = \frac{R_2}{20} = \frac{10k\Omega}{20} = 500\Omega$ (use 470Ω)

$R_3 = R_2 = 10k\Omega$

$V_{cc} \geq (V_0 + 3V) = \pm(5V + 3V)$

$\geq \pm 8V$.

Circuit

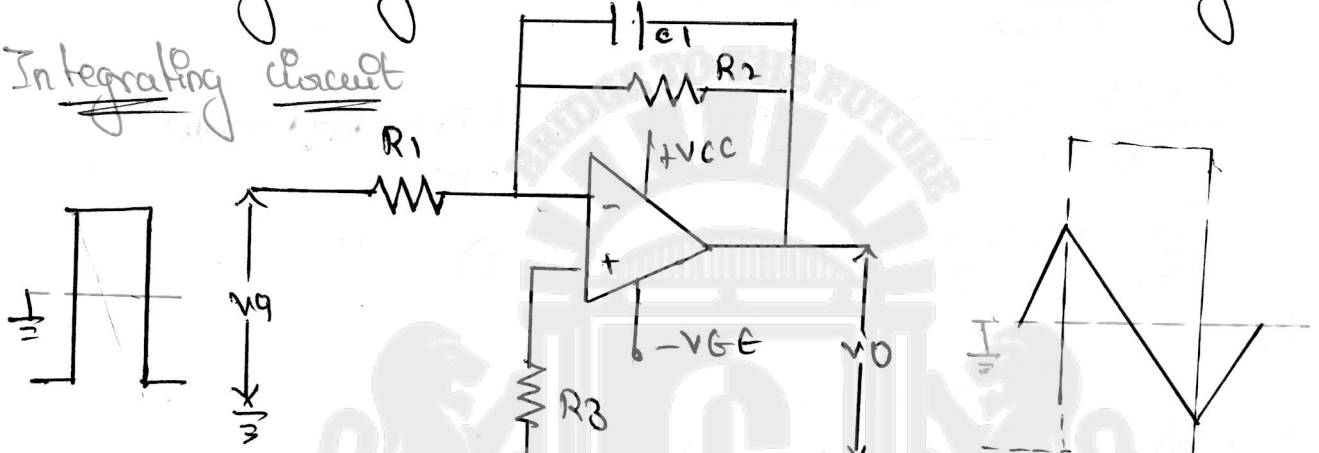


$\Rightarrow A_0 = \frac{R_2}{R_1} = \frac{10k\Omega}{470\Omega} = 21$

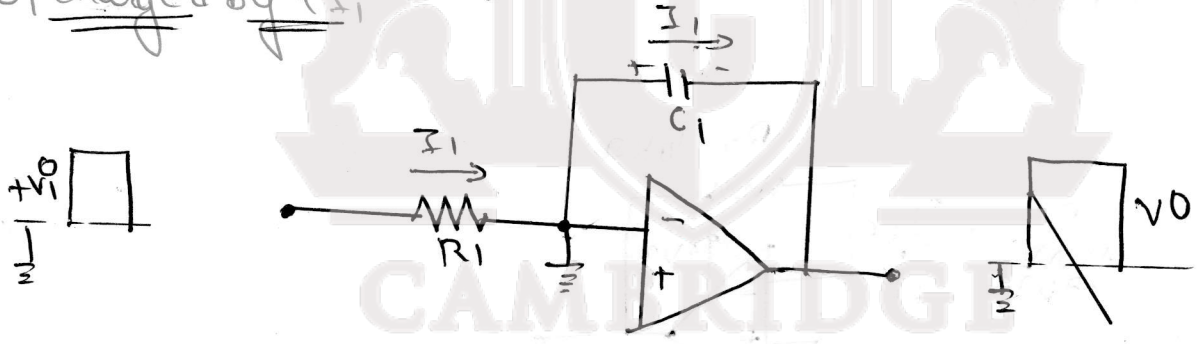
⇒ Integrating circuit:-

An integrating circuit produces an output voltage which is proportional to the area contained under the input waveform. Integration can be performed by a simple RC circuit. But use of an OP-AMP provides a much lower output resistance and higher output voltage than is possible with RC circuit. The integrating circuit resembles an inverting amplifier

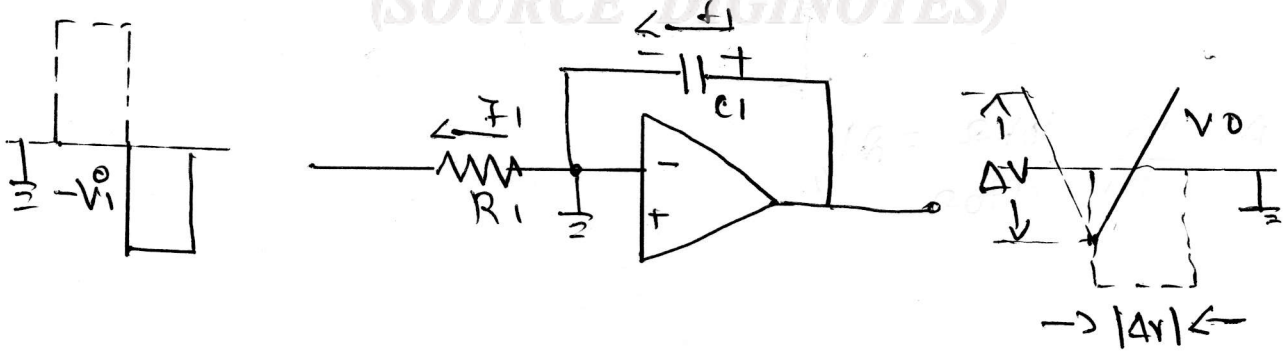
i) Integrating circuit



ii) C_1 charged by $+I_1$



iii) C_1 charged by $-I_1$



⇒ During the positive half cycle of a square wave input, current I_1 is a constant quantity flowing into R_1.
When I_1 much larger than the OPAMP input bias current, effectively all of I_1 flows to R_2 and C_1.
The Resistance R_2 is so high that virtually all of I_1 flows through the capacitor. So I_1 charges. Since the input current is constant, the capacitor is charged linearly and the output is negative-going ramp.

⇒ During the negative half cycle of the square wave input, the direction of I_1 is reversed. The capacitor is now linearly charged negative on the left and positive on the right.
Thus it generates a triangular output waveform which is negative going when the input is positive and positive going when the input is negative.

⇒ The output peak voltage is summation. (Integration of the input).

Design:- $C_1 = \frac{I_1 \Delta t}{\Delta V}$ $\quad \Delta t \rightarrow$ ramp time, $\Delta V \rightarrow$ peak to peak amplitude.

$$\therefore R_1 = \frac{V_i}{I_1}$$

$$R_2 = 20R_1$$

$$R_3 = R_2 \| R_1 \approx R_1$$

At high frequencies, capacitor C_1 behaves as a short circuit, giving 100% feedback. So, for frequency compensation purposes the circuit should be treated as a voltage follower.

Problem.

Using a BIFET OPAMP design an integrating circuit to produce a triangular output waveform with a peak-to-peak amplitude of 4V. The input is a ±5V square wave with a frequency of 500Hz.

Sol

$C_1 >>$ Stray capacitance

$C_1 = 0.1\mu f$ (Standard value)

$$\Delta t = \frac{T}{2} = \frac{1}{2f}$$

$$= \frac{1}{2 \times 500Hz} = 1ms$$

$\Delta V = 4V.$

$$I_1 = \frac{C_1 \Delta V}{\Delta t} = \frac{0.1\mu f \times 4V}{1ms} = 400\mu A$$

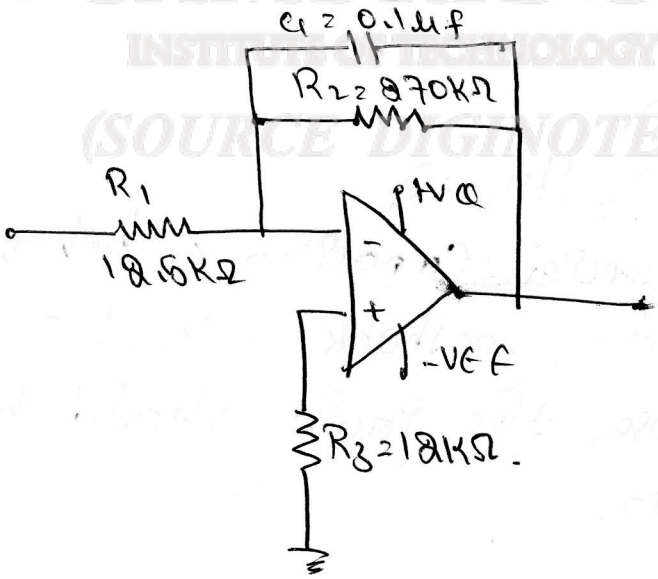
$$R_1 = \frac{V_i}{I_1} = \frac{5V}{400\mu A} = 12.5K\Omega$$ (use a $12K\Omega$ standard value with a 470Ω connected in series)

$R_2 = 20R_1 = 20 \times 12.5K\Omega$

$= 250K\Omega$ (use a $270K\Omega$ standard value)

$R_3 = R_1 = 12.5K\Omega$ (use a $12K\Omega$ standard value)

Circuit:-



PHASE SHIFT OSCILLATOR

Circuit operation

- The phase shift Oscillator as shown below consisting of an inverting amplifier and RC phase shift network
- The RC network feeds a portion of the amplifier ac output back to the amplifier input.
- The amplifier has an internal phase shift of $-180°$ and the phase shift network provides $+180°$ of phase shift. So, the signal fed back to the input can be amplified to reproduce the output. The circuit is then generating its own input signal, which means it is oscillating
- For oscillations to be sustained in any sinusoidal oscillator, certain conditions, known as the Barkhausen criteria, must be fulfilled. These are that the loop gain around the circuit must be equal to (or greater than) one, and the phase shift around the circuit must be zero.

- The RC network connected between the amplifier output and input terminals consists of three resistors and three capacitors. Resistor R_1 functions as the last resistor in the phase shift network and as the amplifier input resistor. The phase shift network illustrated is a phase lead network. This produces a $+180^\circ$ phase shift, so the total phase shift around the loop is $(-180^\circ + 180^\circ) = 0^\circ$. A phase lag network would work just as well, giving a total loop phase shift of $(-180^\circ - 180) = -360^\circ$

- The frequency of the Oscillator output depends on the capacitor and resistor values employed in the phase shift network. If three equal-value resistors and three equal value capacitors are used, the RC circuit can be analyzed to show that the network phase shift is 180° when

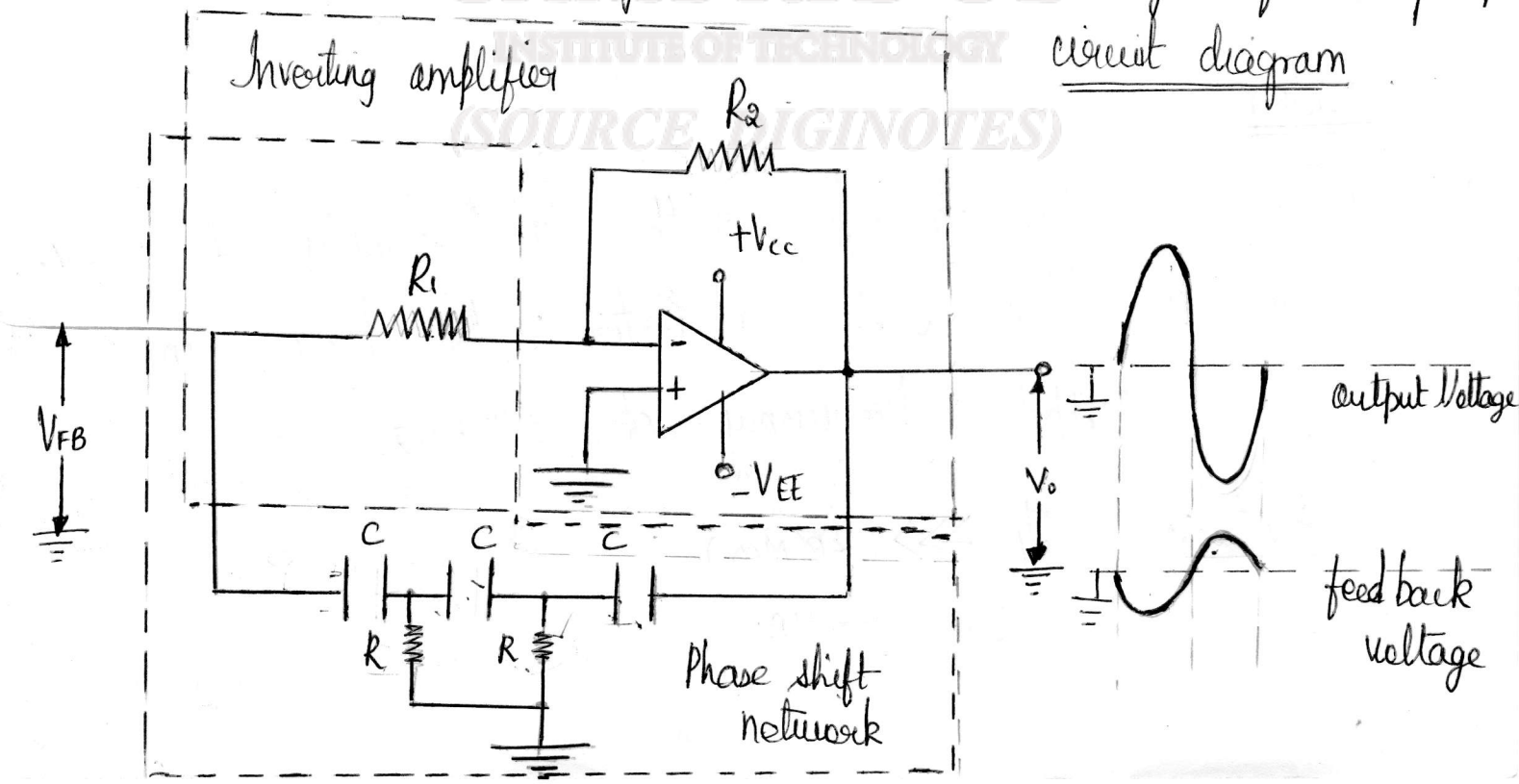
$$X_C = \sqrt{6}\,R$$

This gives an Oscillation frequency of,

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

- In addition to providing network phase shift, the RC network attenuates the amplifier output. Network analysis shows that at the required 180° phase shift the RC network has an attenuation factor of 29. This means, that the amplifier must be have a voltage gain of 29 for the loop gain to equal 1
- If the amplifier gain is less than 29, the circuit will not oscillate. When the gain is substantially greater than 29, the oscillator output waveform is likely to be distorted. A gain just slightly greater than 29 gives a reasonably undistorted sinusoidal waveform. In the absence of amplitude stabilization, the output peaks will approach the positive and negative saturation voltages of the op-amp.

circuit diagram



Phase shift Oscillator Design

Design of a phase shift Oscillator commences with design of the inverting amplifier to have a voltage gain just slightly greater than 29. The phase shift network resistors are then made equal to the amplifier input resistor R_1 and the network capacitance is determined. where an Uncompensated op-amp is used, frequency compensating components should be included. if the desired oscillating frequency is much lower than the frequency at which instability might occur, the circuit can usually be heavily over-compensated.

Problem

1. Using a 741 op-amp with a supply of ±12V, design a phase shift oscillator to have an output frequency of 3.5 KHZ

Solution: WKT. $I_1 \ggg I_{B(Max)}$

$I_1 = 50\mu A$

18

$$V_o \simeq \pm (V_{cc} - 1V) \simeq \pm(12V - 1V)$$
$$\simeq \pm 11V$$

$$R_2 = \frac{V_o}{I_1} = \frac{11V}{50\mu A}$$

$= 220k\Omega$ (standard value)

$$R_1 = \frac{R_2}{A_o} = \frac{220k\Omega}{29}$$

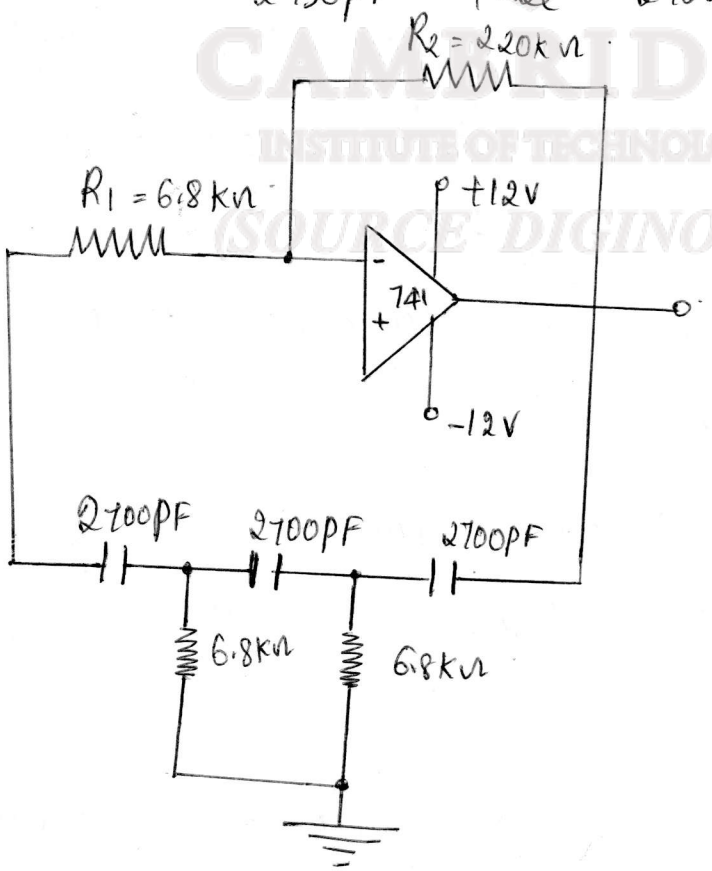
$= 7.6k\Omega$ (use $6.8k\Omega$ to give $A_o > 29$)

$$R = R_1 = 6.8k\Omega$$

w.k.t

$$C = \frac{1}{2\pi R f \sqrt{6}} = \frac{1}{2\pi \times 6.8k\Omega \times 3.5kHz \times \sqrt{6}}$$

$= 2730pF$ (use 2700 pF standard value).



WEIN BRIDGE OSCILLATOR

Circuit operation

A wein bridge is an ac bridge in which balance is obtained only when the Supply voltage has a particular frequency. In the wein bridge oscillator the resistive and capacitive components constitute a wein bridge. The output of the bridge is applied to the op-amp input terminals, and the op-amp output provides ac Supply to the bridge.
Another way of looking at the circuit is that the op-amp together with Resistors R_3 and R_4 is a non-inverting amplifier, and the other Components are a feedback network. The output voltage from the amplifier is attenuated but not phase shift by the feedback network, and the feedback voltage is amplified to produce the output.

The Barkhausen criteria for Zero loop phase shift is fulfilled, in this case, by the amplifier and the feedback network each having Zero phase shift This occurs at only one particular frequency, the

resonant frequency of the bridge. At the other frequencies, the bridge output and feedback voltages do not have the correct phase shift or amplitude relationship to sustain oscillations.

Analysis of the bridge circuit reveals that balance is obtained when the following two are fulfilled.

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

and

$$2\pi f = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

if $R_1 = R_2$ and $C_1 = C_2$ then,

$$f = \frac{1}{2\pi CR}$$

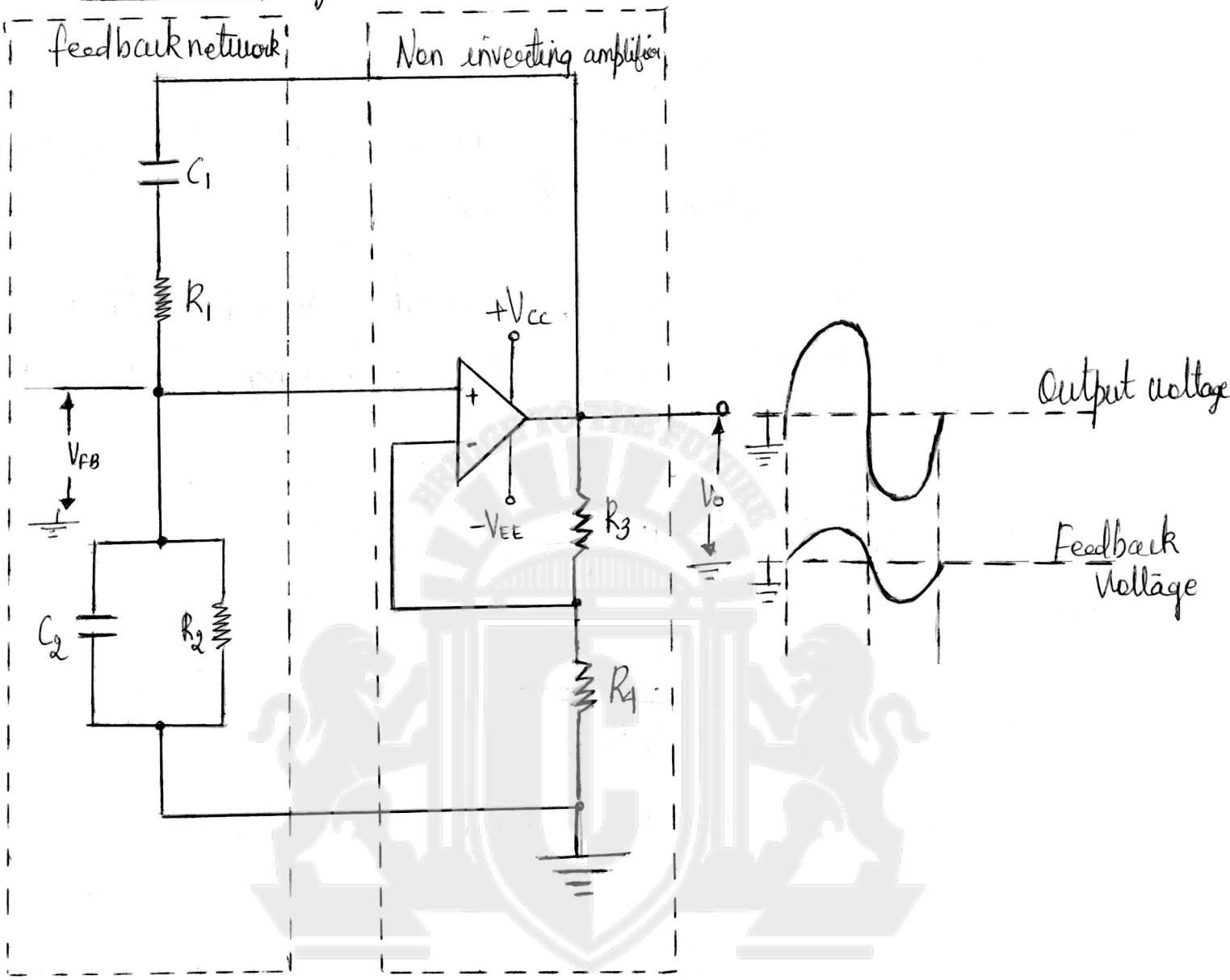
$$R_3 = 2R_4$$

The amplifier voltage gain is

$$A_0 = \frac{R_3 + R_4}{R_4} = 3$$

The feedback network attenuates the amplifier output by a factor of 3, so the voltage gain of the noninverting amplifier must be a minimum of 3 to sustain oscillations

circuit diagram



Wein bridge Oscillator Design

A wein bridge oscillator is designed by it first determining the non-inverting amplifier components in the usual way. Then, R_1 and R_2 are usually made equal to R_4, and the capacitor values are determined. If a BIFET op-amp is used, it is best to start by selecting a capacitance value very much larger than stray capacitance.

Problem:

1. Using a BIFET op-amp with a Supply ±12V, design a Wein bridge Oscillator to have an output frequency of 15KHZ

Solution.

Select, $C = C_1 = C_2 = 0.01\mu F$

W.K.T $R = \dfrac{1}{2\pi C f} = \dfrac{1}{2\pi \times 0.01\mu F \times 15KHZ}$

$= 1.06\,K\Omega$ (use $1K\Omega$ standard value).

$R_1 = R_2 = R = 1K\Omega$

let, $R_4 = R_2 = 1K\Omega$

for $A_0 = 3$ $R_3 = 2R_4 = 2 \times 1K\Omega$

$= 2K\Omega$ { Use $2.2K\Omega$ standard value to give $A_0 > 3$ }

CROSSING DETECTORS:-

Zero crossing Detector:-

→ The zero crossing detector circuit is simply an op-amp with the inverting input terminal grounded & the i/p signal applied to the non-inverting input.

→ When the input is above the ground level, the output is saturated at its positive maximum, & when the i/p is below the ground level, the o/p is at its negative maximum level.

→ This is illustrated by the i/p & o/p waveforms, which shows that the output voltage changes from one extreme to the other each time the i/p voltage crosses zero. as shown in fig.1(b)

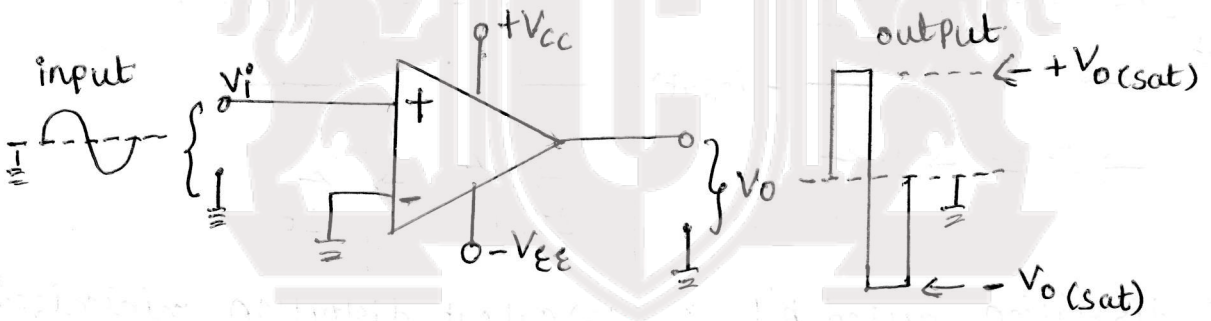


fig.1 (a) Non-inverting zero crossing detector.

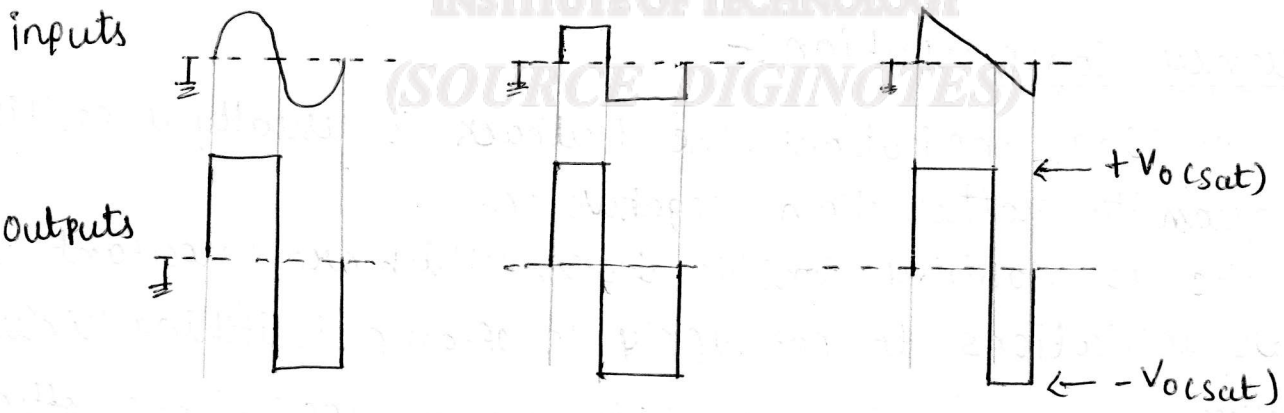


fig.1 (b) Input & output waveforms.

→ Because the output voltage from the circuit in fig.1(a) always moves in a positive direction when the input crosses zero from negative to positive, the circuit can

be classified as a non-inverting zero crossing detector.

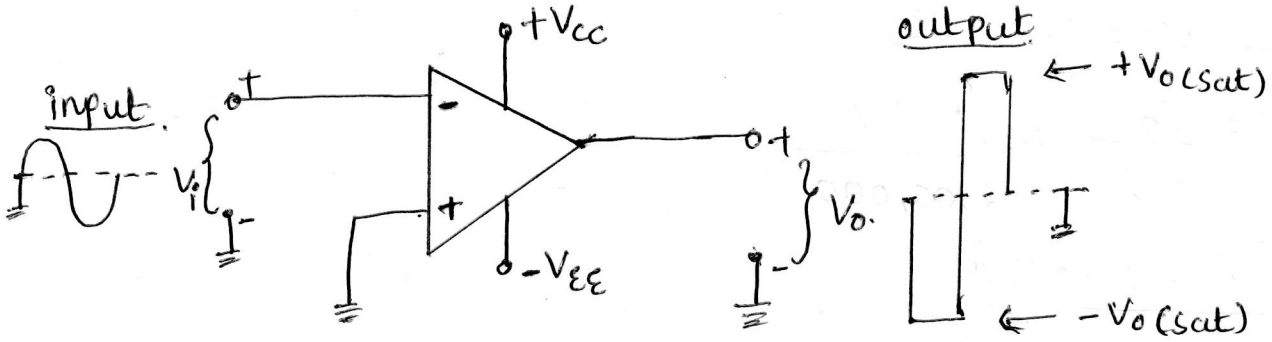


fig 1.(c) Inverting zero-crossing detector & i/p & o/p wave-forms

→ If the op-amp non-inverting i/p is grounded & the signal is applied to the inverting input as in fig.1(c), the output is negative when the i/p is above the ground level & vice versa.

→ Because of the waveform inversion, this circuit is an inverting zero crossing detector, also referred to as an inverter.

Problem:-

① If the zero-crossing detector in fig.1(c) uses a 741 op-amp with a ±15V supply, determine the typical o/p voltage swing & the typical i/p voltage level above & below the ground level at which the o/p switches. Also calculate the rise time of the o/p voltage.

Sol^n:- $\Delta V_o = (V_{CC} - 1V) - (V_{EE} + 1V) =$

$= (15V - 1V) - (-15V + 1V)$

$= 28V$

$\Delta V_o = \pm 14V$

For the 741,

$A_V = 2,00,000$ (typical)

Slew rate $= 0.5\ V/\mu s$

$$V_i = \frac{V_o}{A_V} = \frac{\pm 14\ V}{2,00,000}$$

$$\boxed{V_i = \pm 70\ \mu V}$$

$$\Delta t = \frac{\Delta V_o}{SR} = \frac{28\ V}{0.5\ V/\mu s}$$

$$\boxed{\Delta t = 56\ \mu s}$$

Voltage level detector:-

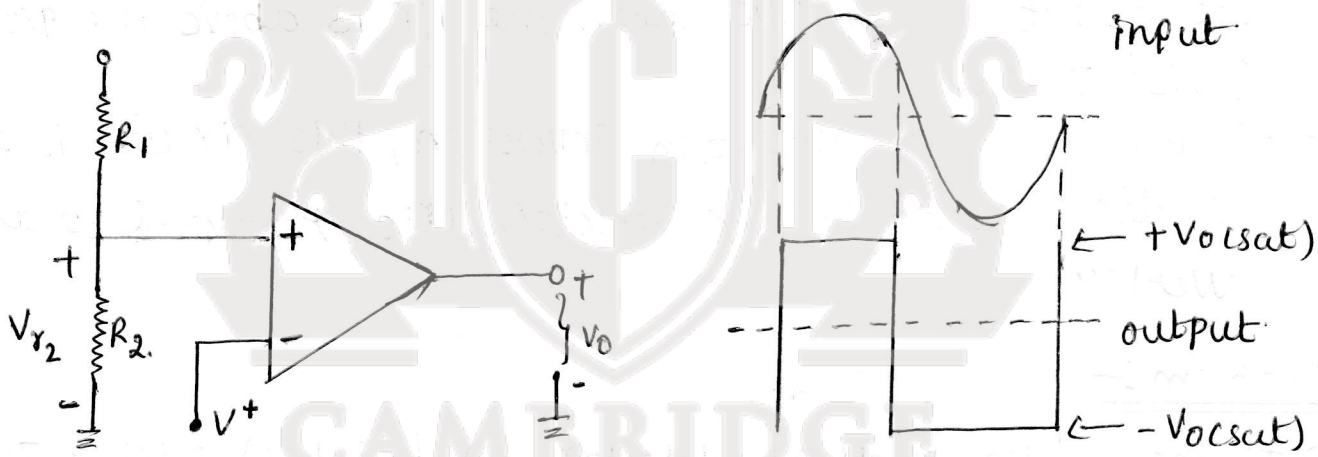


fig (2)

-> The circuit in fig(2) has the op-amp inverting i/p biased to a positive level via a voltage divider (R_1 & R_2). The bias voltage level (V_{r_2}) could be a negative quantity instead of positive.

-> The waveforms show that the o/p voltage switches levels when the i/p voltage crosses the bias voltage level. This circuit is appropriately named a voltage level detector.

-> voltage level detectors & zero crossing detectors are sometimes reffered to as comparators because the i/p voltage at one terminal is being compared to the i/p voltage at the other input terminal.

Capacitor - Coupled crossing Detector:-

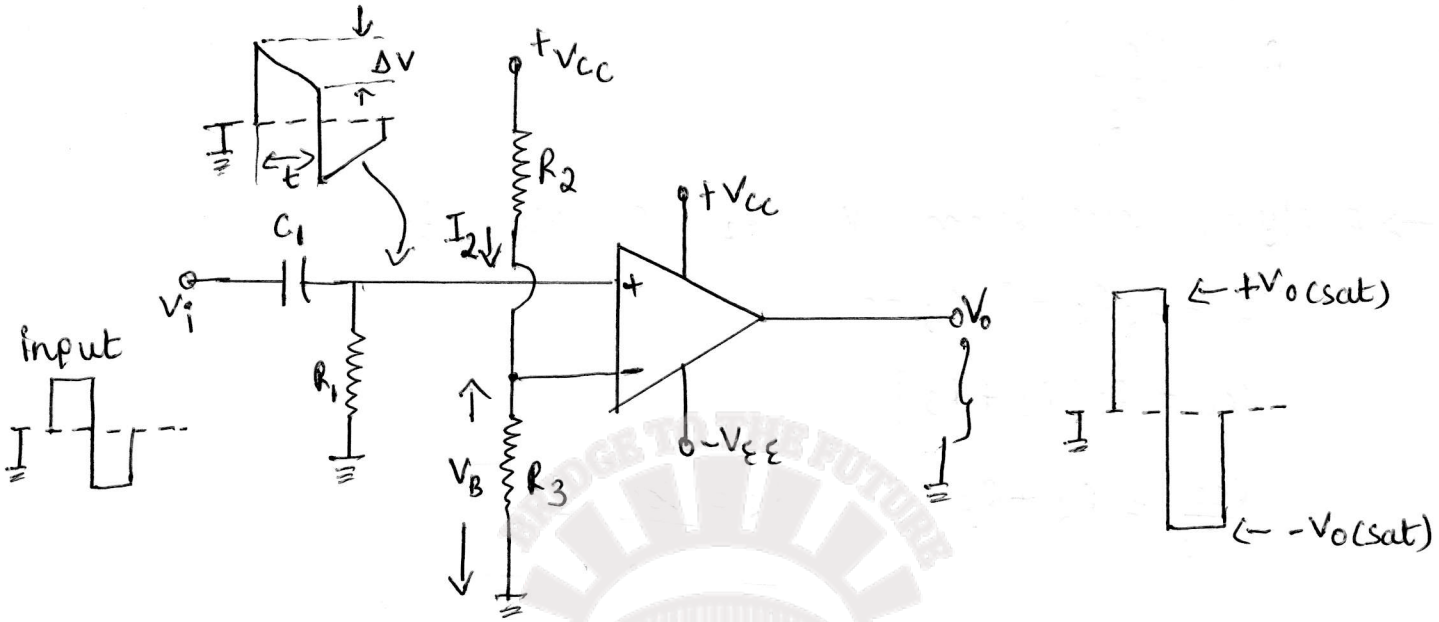


fig (a) capacitor coupled crossing detector

-> Fig (a) shows capacitor coupled crossing detector with Non-inverting terminal connected to ground via resistor R_1 to provide a dc bias current path to the op-amp.

-> The inverting terminal connected to a potential divider circuit. Due to this inverting terminal is held at a small +ve voltage (V_b). This ensures that the o/p is held at $-V_{sat}$, when no input signal is present

-> When capacitor-coupled signal (V_i) drives the non-inverting input terminal above V_b, the o/p switches to $+V_{sat}$ & when input is less than V_b (i.e $V_i < V_b$) the o/p falls back to $-V_{sat}$

Design steps:-

-> The resistance R_1 is designed as

$$R_{1(max)} = R_1 = \frac{0.1\, V_{be}}{I_{B(max)}}$$

-> The current I_2 is choosen to be about 100 times $I_{B(max)}$

$$\therefore \boxed{I_2 = 100\, I_{B(max)}}$$

-> The Voltage V_B across R_3 is given by

$$V_B = I_2 R_3$$

$$\boxed{R_3 = \frac{V_B}{I_2}}$$

-> Applying KVL from V_{CC}, R_2 & R_3 we get

$$V_{CC} - I_2 R_2 - I_2 R_3 = 0$$

$$V_{CC} = I_2 [R_2 + R_3]$$

$$\frac{V_{CC}}{I_2} = R_2 + R_3 \qquad \boxed{R_2 = \frac{V_{CC}}{I_2} - R_3}$$

-> At lower frequency, X_{C_1} should be much smaller than R_1

i.e $X_{C_1} = \frac{R_1}{20}$. $\boxed{C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{20}\right)}}$

Due to this, there will be approximately a 2.9° phase shift. This will decrease with increasing signal frequency.

-> The i/p voltage to capacitor 'C_1' may not be symmetrical above or below ground level, but it is always symmetrical on the op-amp side of C_1.

-> when square-wave is applied as an i/p to a capacitor-coupled detector, the waveform at the op-amp i/p terminal can develop considerable tilt as shown in fig (a)

-> The i/p current is calculated as:

$$I_1 = \frac{V_i}{R_1} \qquad \text{where, } t = \frac{1}{2f}$$

Assuming I_1 constant,

$$C_1 = \frac{Q}{V} \qquad C_1 = \frac{I_1 t}{\Delta V}$$

Inverting Schmitt Trigger Circuit :-

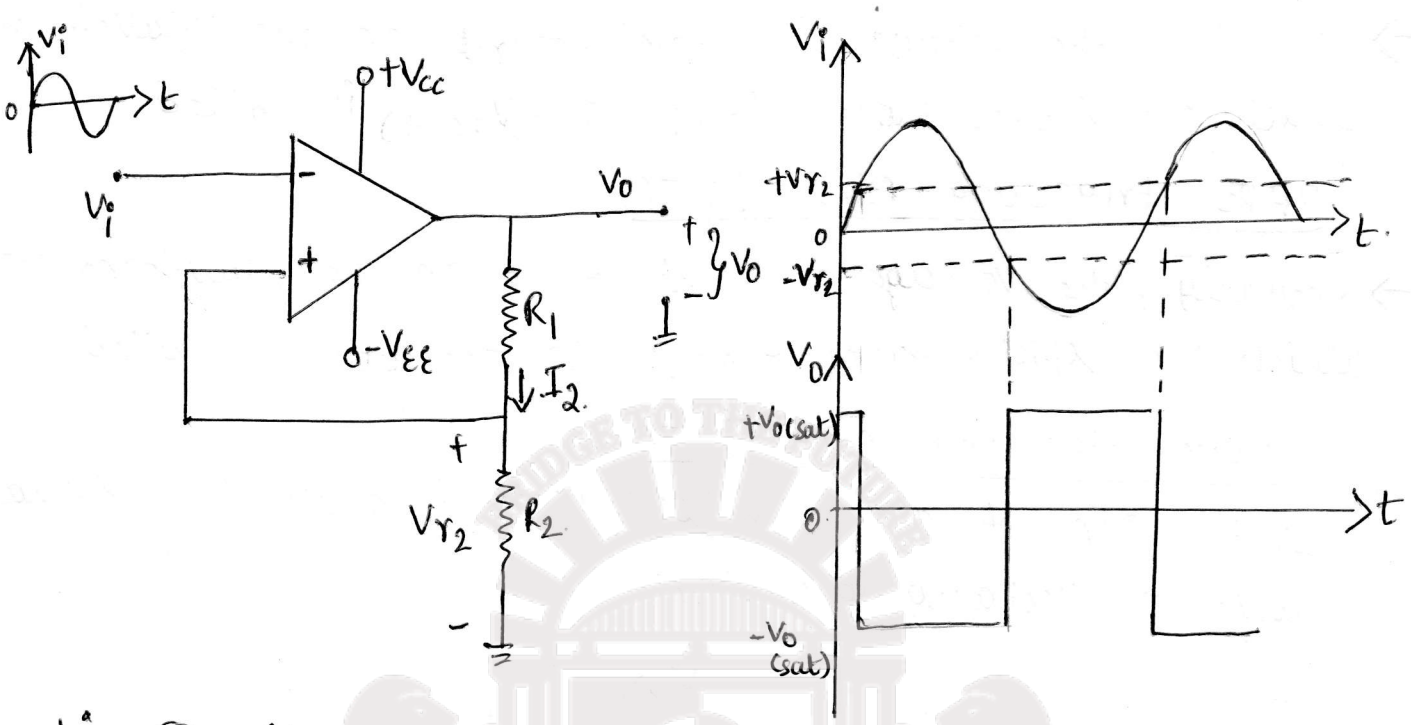


fig (b) Shows an inverting schmitt trigger circuit.

-> The i/p is applied to the inverting terminal of the schmitt trigger circuit. The feedback signal is given to the Non-inverting terminal. This ensures +ve feedback.

-> The voltage at the non-inverting i/p is

$$V_{ref} = I_2 R_2$$

$$I_2 = \frac{V_o}{R_1 + R_2} \quad \therefore \quad \boxed{V_{ref} = \frac{V_o R_2}{R_1 + R_2}}$$

-> when the o/p voltage V_o is at $+V_{sat}$, then V_{ref} will be a Positive voltage & voltage at Non-inverting terminal will also be positive $(+V_{ref})$.

i.e $V_{ref} = \frac{V_o R_2}{R_1 + R_2}$ $\quad \boxed{+V_{ref} = \frac{+V_{o(sat)} R_2}{R_1 + R_2}}$

-> when $V_i > +V_{ref}$, then the voltage at inverting terminal becomes greater than $(+V_{ref})$ Non-inverting terminal & the o/p will switch from $+V_{o(sat)}$ to $-V_{o(sat)}$.

i.e $V_{ref} = \frac{V_o R_2}{R_1 + R_2}$. $\boxed{-V_{ref} = \frac{-V_{o(sat)} R_2}{R_1 + R_2}}$

→ In fig (b), the voltage at point $+V_{ref}$ on the waveform at which o/p shifts from $+V_{o(sat)}$ to $-V_{o(sat)}$ is called "upper triggering point" (UTP)

→ similarly, the voltage at point $-V_{ref}$ on the waveform at which o/p shifts from $-V_{o(sat)}$ to $+V_{o(sat)}$ is called "lower triggering point" (LTP)

Thus the o/p of a schmitt trigger is always a square wave or rectangular wave.

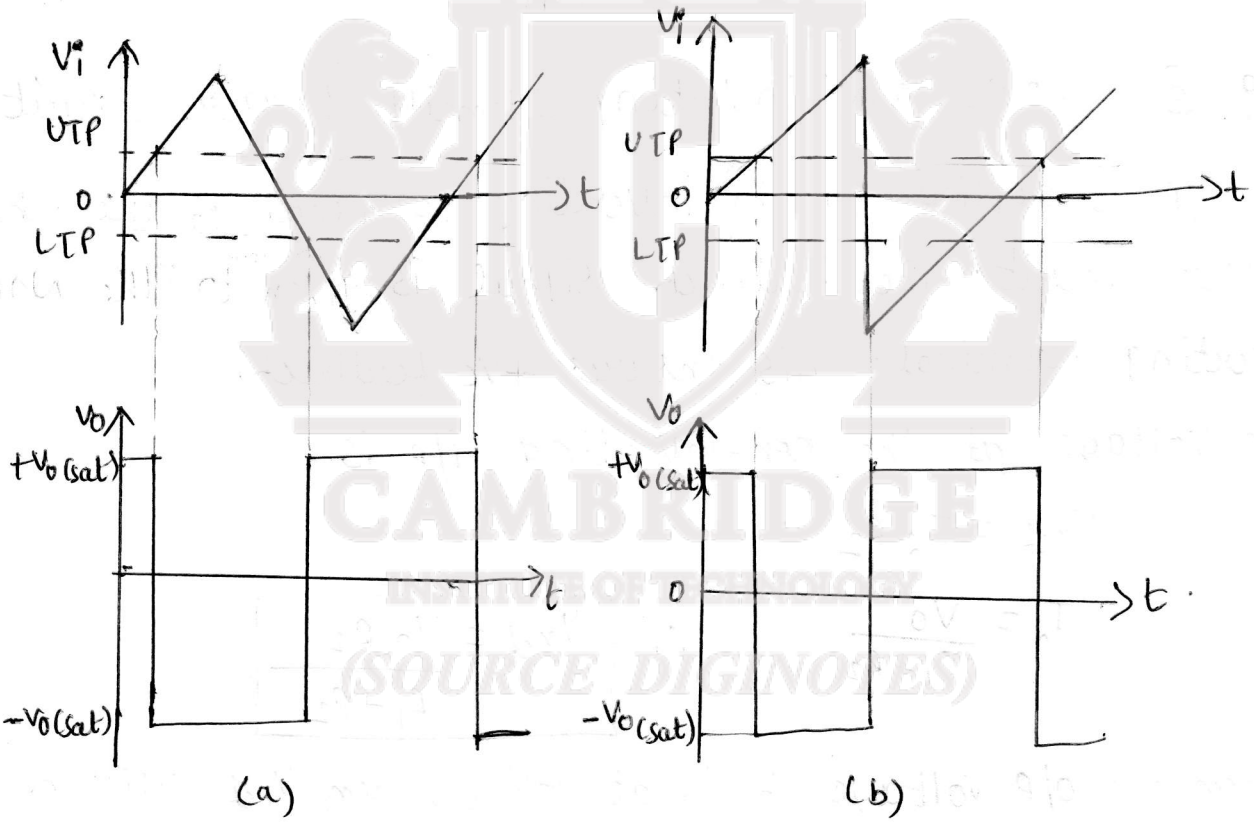
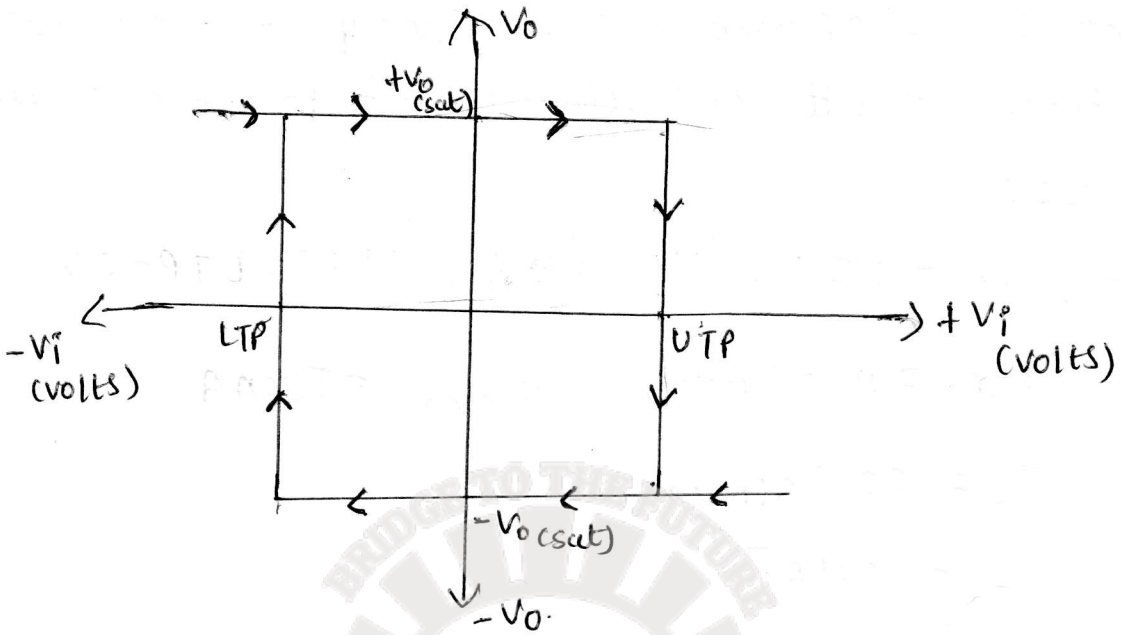


fig (a) Triangular i/p waveform producing square-wave
(b) Saw tooth i/p waveform producing square-wave.

Input/output characteristics or Transfer characteristics:-



* when $V_i = 0V$, the o/p will be at $+V_{o(sat)}$, when $V_i = UTP$, the o/p switches from $+V_{o(sat)}$ to $-V_{o(sat)}$.

  when $V_i < LTP$, the o/p will be at $-V_{o(sat)}$, when $V_i = LTP$, the o/p switches from $-V_{o(sat)}$ to $+V_{o(sat)}$

* The voltage difference between upper & lower triggering points is reffered to as hysteresis

$$\therefore \boxed{V_h = UTP - LTP}$$

Schmitt trigger circuit design:-

-> The current I_2 flowing through the resistors R_1 & R_2 is choosen to be 100 times $I_{B(max)}$

i.e $I_2 = 100\, I_{B(max)}$

-> $R_2 = \dfrac{\text{triggering Voltage}}{I_2}$.

-> $R_1 = \dfrac{V_o - \text{triggering voltage}}{I_2}$.

Problems:-

(1) using a 741 op-amp with a supply of ±12V, design an inverting- schmitt triggering circuit to have trigger points of ±2V.

given:- $V_{cc} = +12V$, $V_{sat} = 12V$, $UTP = LTP = 2V$

sol^n:- For 741 op-amp, $I_{B(max)} = 500nA$

$I_2 = 100\, I_{B(max)}$

$\boxed{I_2 = 50\mu A}$

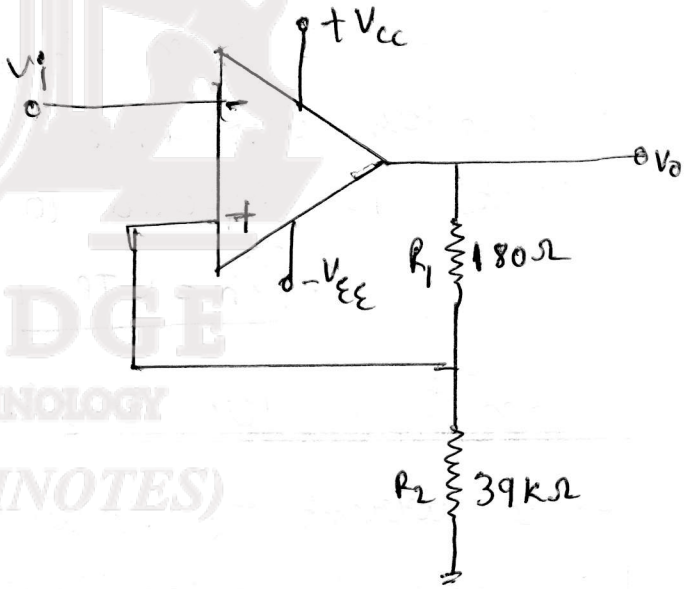
* $\boxed{V_{R2} = UTP = 2V}$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{2}{50\mu} = 40K\Omega$

choose $\boxed{R_2 = 39K\Omega}$

* $I_2 = \frac{V_{R2}}{R_2} = \frac{2V}{39}$

$\boxed{I_2 = 51.3\mu A}$



* $R_1 = \frac{V_o(sat) - V_{R2}}{I_2} = \frac{12-2}{51.3\mu}$

$R_1 = 175\Omega$

choose $\boxed{R_1 = 180\Omega}$

Adjusting the Trigger Points (UTP & LTP) :-

① Schmitt trigger with LTP = 0 :-

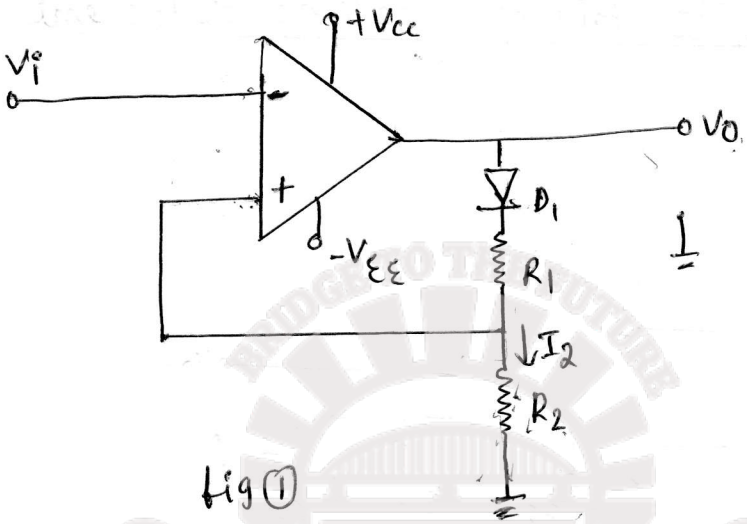


fig ①

→ fig ① shows the circuit with +ve UTP & zero LTP. This can be achieved by using a diode in series with R_1

→ When the o/p is at $+V_{o(sat)}$, the diode D_1 is forward biased & UTP will be equal to the voltage drop across resistor R_2. (i.e $V_{ref} = UTP$)

$$UTP = IR_2$$

where, $\beta = \frac{R_2}{R_1 + R_2}$

$$\boxed{UTP = \frac{V_{o(sat)} R_2}{R_1 + R_2}}$$

→ When the o/p is at $-V_{o(sat)}$, the diode D_1 is reverse biased & only a very small i/p bias current (I_B) flows through R_2 & the non-inverting terminal is held at ≈0V. thus LTP = 0.

→ When the i/p voltage is reduced below ground level, the o/p will go to $+V_{sat}$.

→ The Diode D_1 must be selected to have a maximum reverse voltage greater than the circuit supply voltage

→ The maximum reverse recovery time "t_{rr}" should be much smaller than the minimum pulse width of the i/p signal i.e

$$t_{rr} \leq \frac{\text{minimum pulse width}}{10}$$

② Inverting schmitt trigger having different LTP & UTP :-

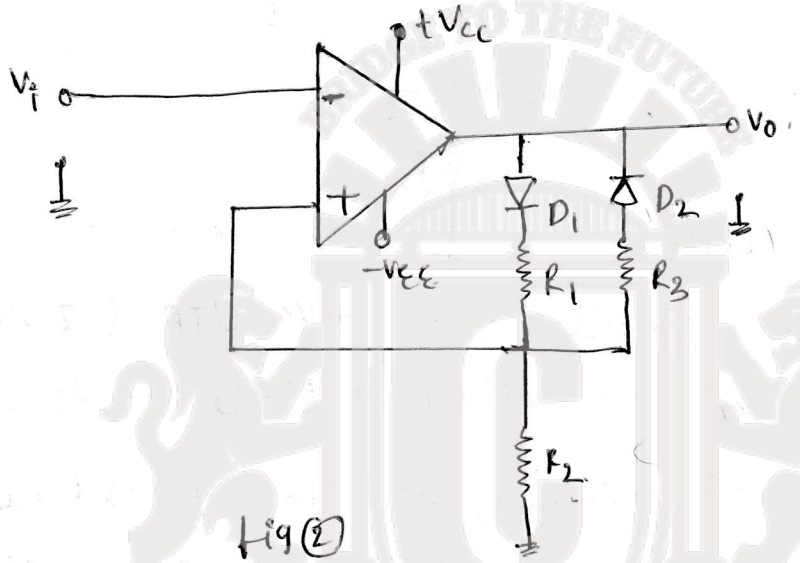


fig ②

→ The circuit diagram shown in fig ② uses two Diodes D_1 & D_2 & 3 Resistors R_1, R_2 & R_3 to get different LTP & UTP Voltages.

Case (i): when $V_o = +V_{o(sat)}$, the diode D_1 is forward biased & D_2 is reverse biased. The UTP is given by

$$\boxed{UTP = \frac{[|V_o| - V_F]\, R_2}{R_1 + R_2}}$$

Case (ii): when $V_o = -V_{o(sat)}$, the diode D_1 is reverse biased & D_2 is forward biased. The LTP is given by

$$\boxed{LTP = V_{R_2} = \frac{[|V_o| - V_F]\, R_2}{R_3 + R_2}}$$

where, V_F is the voltage drop across D_1 & D_2

* Different values of R_1 & R_2 gives different UTP & LTP voltages.

Problems :-

① An inverting schmitt trigger circuit is to have UTP = 2.5V & LTP = 0V. Design a suitable circuit using a bipolar & a ± 18V supply.

Soln :-

given: UTP = 2.5V , LTP = 0V, V_{cc} = 18V

Assume V_F = 0.7V , I_2 = 500 μA

$$R_2 = \frac{V_{R2}}{I_2} = \frac{UTP}{I_2} = \frac{2.5V}{500\mu} = 5K\Omega$$

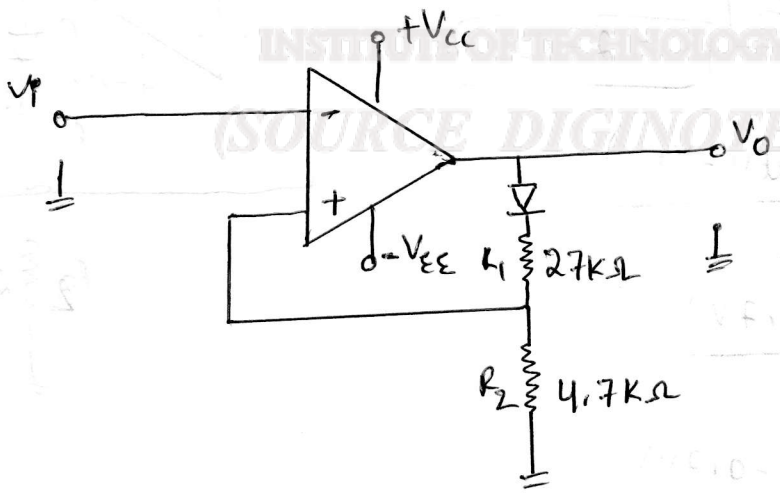
choose $\boxed{R_2 = 4.7K\Omega}$ Now, $I_2 = \frac{V_{R2}}{R_2} = \frac{2.5}{4.7K}$.

$\boxed{I_2 = 532\mu A}$

$$* \; R_1 = \frac{((V_{cc}-1) - V_F) - V_{R2}}{I_2}$$

$$= \frac{17 - 0.7V - 2.5V}{532\mu A} = 25.9k\Omega$$

choose $\boxed{R_1 = 27K\Omega}$



② using a bipolar op-amp with ±18V supply design an inverting schmitt trigger circuit to have UTP = 1.5V & LTP = -3V.

given:- $V_{CC} = 18V$, $-V_{EE} = -18V$, $UTP = 1.5V$ $|LTP| = 3V$

Assume $V_F = 0.7V$

$V_{R_2} = UTP = 1.5V$.

$+V_{o(sat)} = V_{CC} - 1 = 17V$

$-V_{o(sat)} = -V_{EE} + 1 = -17V$

$-V_{o(sat)} = -17V$

* let $I_2 = 500\mu A$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{1.5}{500\mu A} = 3k\Omega$.

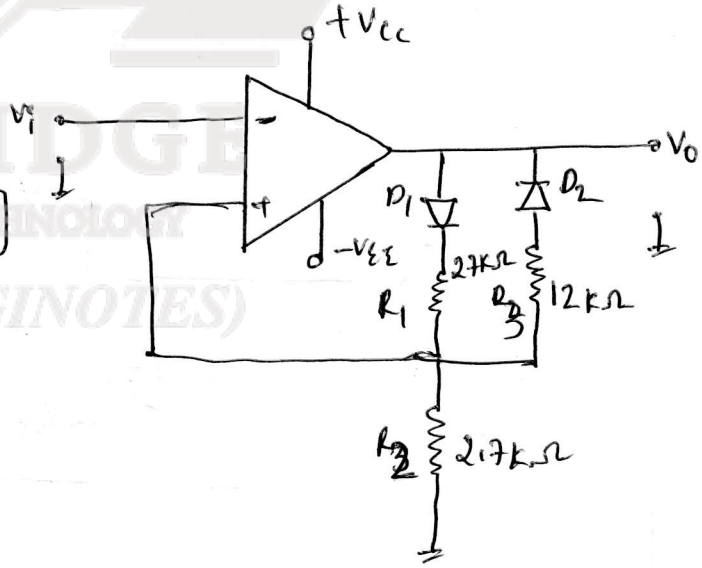
Choose $\boxed{R_2 = 2.7k\Omega}$

* $UTP = \frac{R_2(+V_{o(sat)} - V_F)}{R_1 + R_2}$.

$R_1 + 2.7k\Omega = \frac{2.7k\Omega(17 - 0.7)}{1.5k\Omega}$.

$R_1 = \frac{44.01k}{1.5} - 2.7k\Omega$.

$\boxed{R_1 = 26.64k\Omega}$ choose, $\boxed{R_1 = 27k\Omega}$



* $|LTP| = \frac{R_2(|-V_{o(sat)}| - V_F)}{R_2 + R_3}$

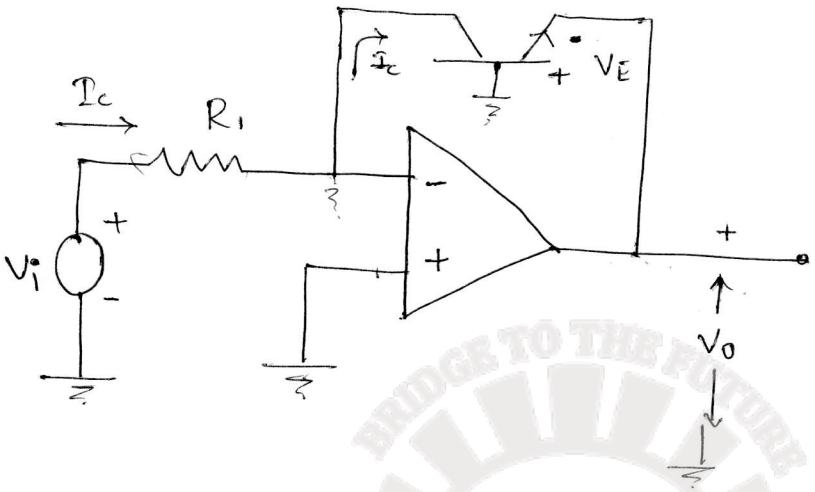
$3 = \frac{2.7k\Omega(17 - 0.7V)}{2.7k + R_3}$.

$2.7k + R_3 = \frac{2.7k\Omega(17 - 0.7V)}{3}$.

$R_3 = \frac{2.7k\Omega(17 - 0.7)}{3} - 2.7k$

$R_3 = 11.97k\Omega$, choose $\boxed{R_3 = 12k\Omega}$

Log and Antilog Amplifier



a) Fundamental log-amp circuit

* The fundamental log-amp circuit is shown in fig (a) where a grounded base transistor is placed in the feedback path.

* Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_S \left(e^{qV_E/kT} - 1\right)$$

Since, $I_C = I_E$ (for grounded base transistor)

$$\therefore \quad I_C = I_S \left(e^{qV_E/kT} - 1\right)$$

I_S = emitter saturation current $\simeq 10^{-13}$ A.
k = Boltzmann's const.
T = absolute temp (in °K)

$$\frac{I_c}{I_s} = (e^{qV_E/kT} - 1)$$

$$e^{qV_E/kT} = \frac{I_c}{I_s} + 1$$

$[\ I_c >> I_s\ ]$

$$e^{qV_E/kT} = \frac{I_c}{I_s}$$

Taking natural log on both sides

$$V_E = \frac{kT}{q} \ln\left(\frac{I_c}{I_s}\right)$$

Also in fig (a) $I_c = \frac{V_i}{R_1}$

$$V_E = -V_0$$

$$\therefore\ V_0 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right)$$

$[\ V_{ref} = R_1 I_s\ ]$

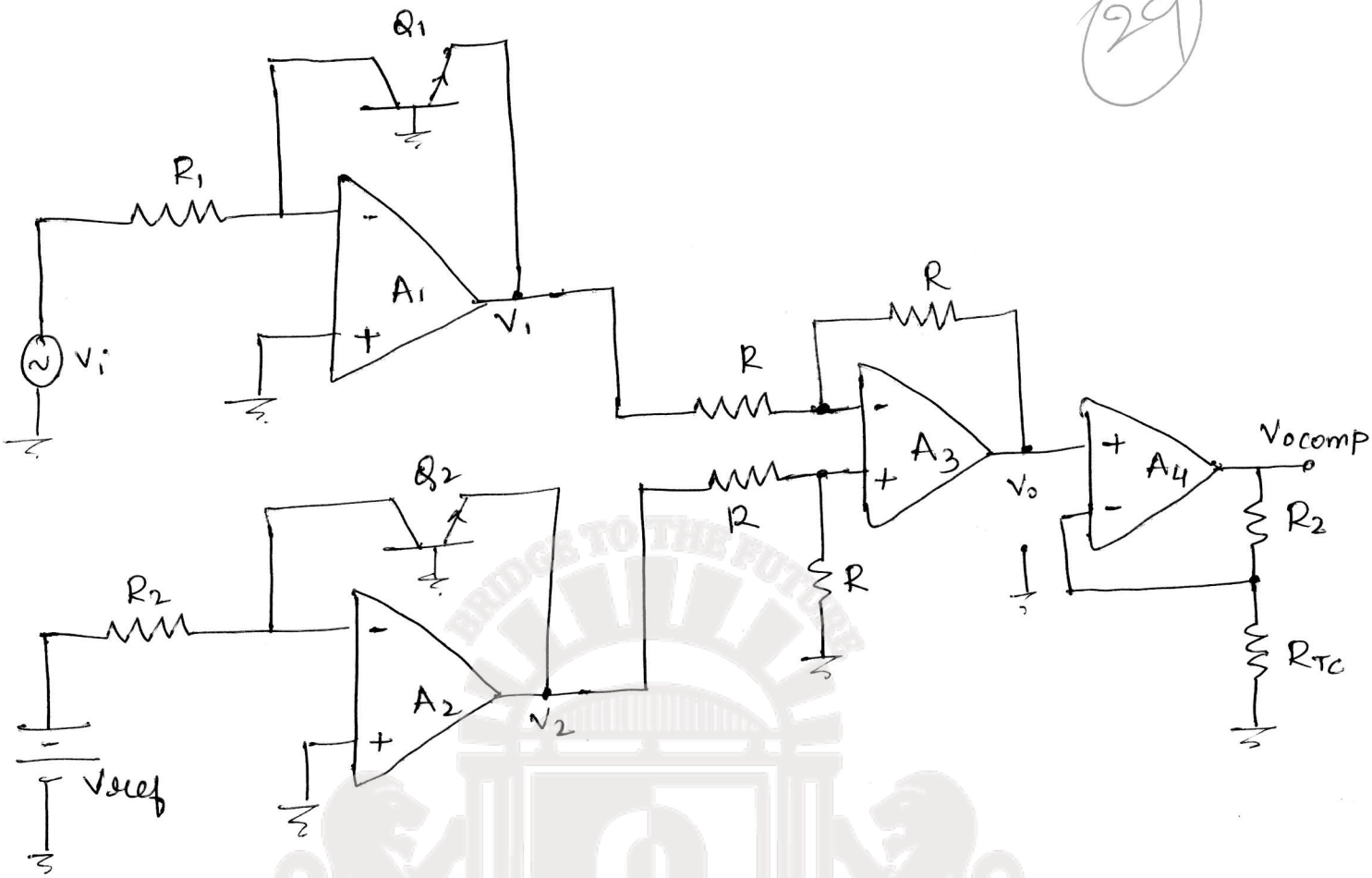
$$\boxed{V_0 = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)}$$

O/P voltage is proportional to logarithm of i/p voltage. $\log_{10} X = 0.4343 \ln X$.

I_s varies from transistor to transistor

$\therefore$ V_{ref} cannot be obtained.

The input is applied to one log-amp while reference voltage is applied to another log-amp.



b) Log-amp with saturation current and temperature compensation.

Assume, $I_{S_1} = I_{S_2} = I_S$

and then $V_1 = -\frac{KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right)$

and $V_2 = -\frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$

$$V_0 = V_2 - V_1$$

$$= \frac{KT}{q}\left[\ln\left(\frac{V_i}{R_1 I_S}\right) - \ln\left(\frac{V_{ref}}{R_1 I_S}\right)\right]$$

$$V_0 = \frac{KT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

The reference level is now set with a single external voltage source. Dependence on device and temperature has been removed.

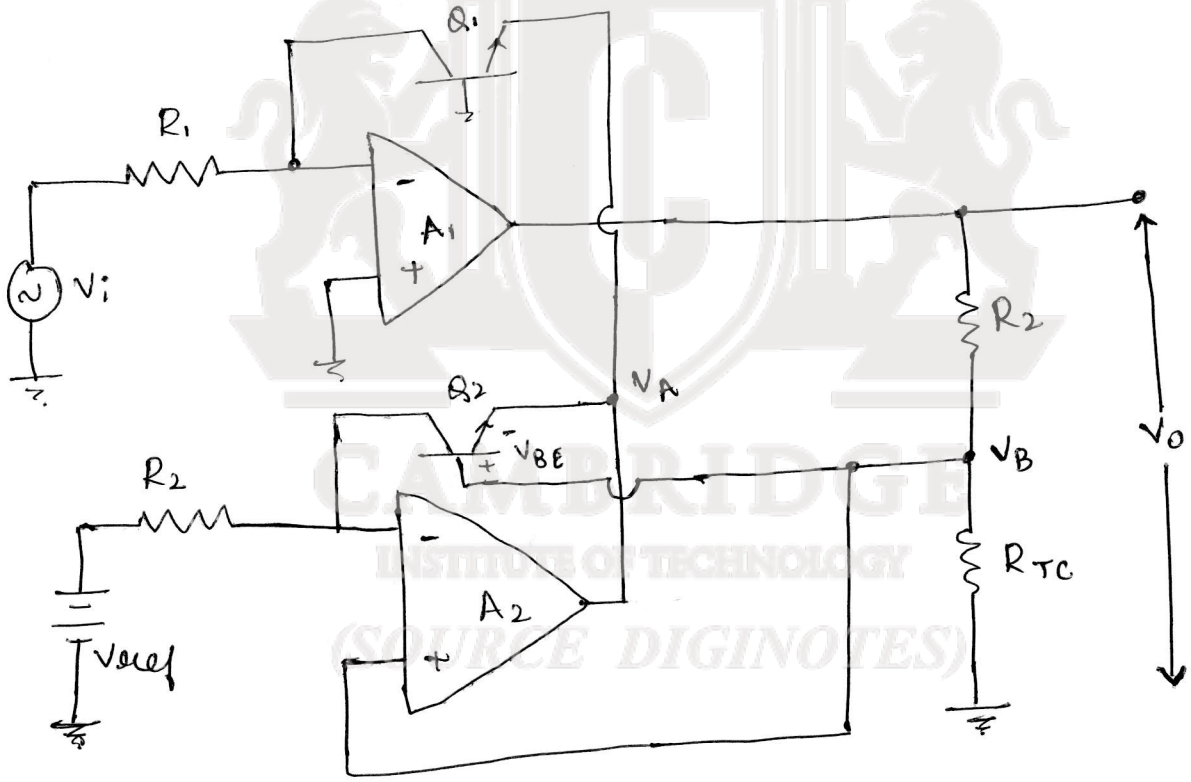
The voltge V_o is still dependent upon temperature and is directly proportional to T.

The output voltage is,

$$V_{ocmp} = \left[1 + \frac{R_2}{R_{TC}}\right] \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

Where,

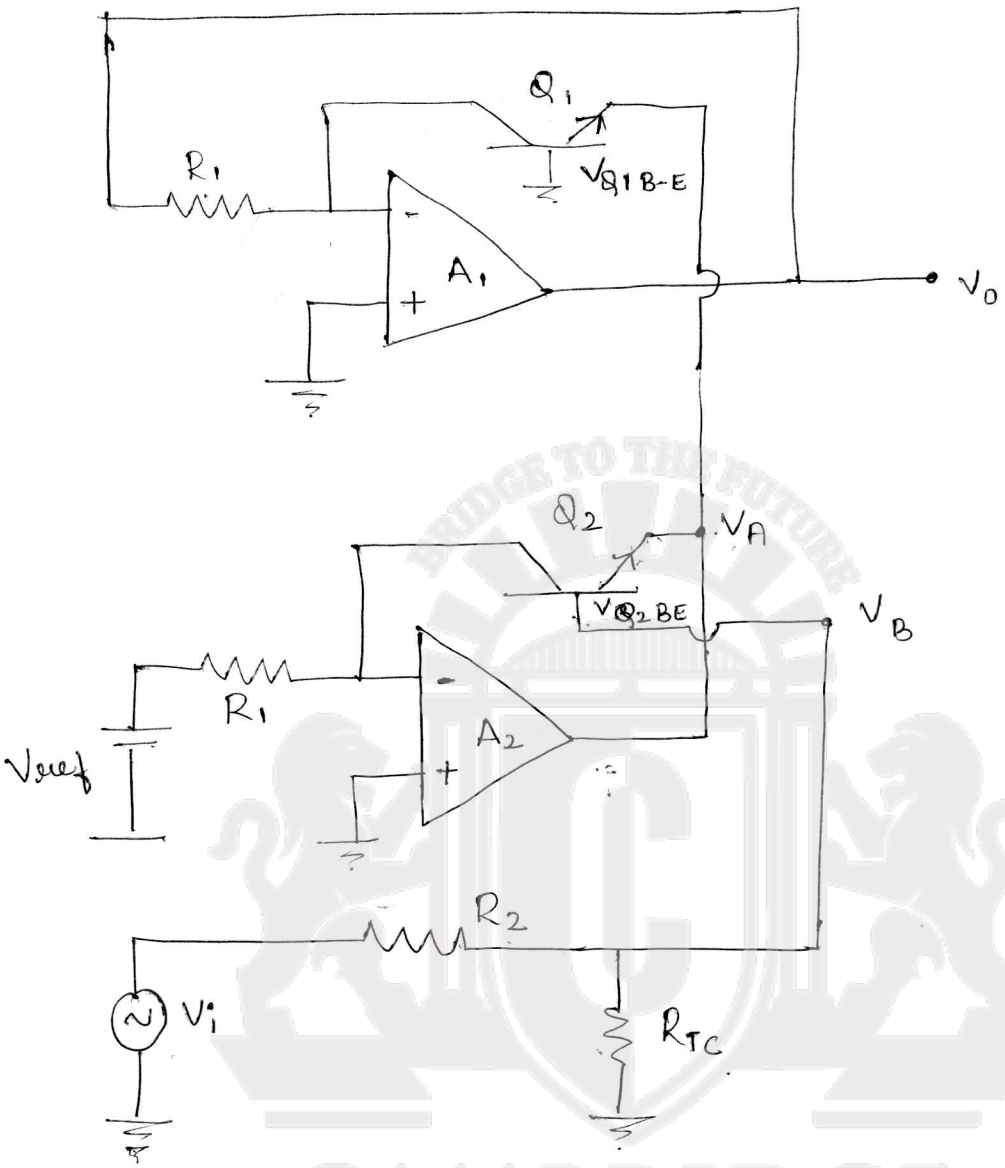
$R_{TC} \rightarrow$ Temperature sensitive resistance.



c) Log-amp using 2-opamps only

fig b) requires 4-opamps and becomes expensive if FET op-amps are used for precision. The same output can be obtained by the circuit of fig c) using 2-opamps only.

Antilog Amplifier



a) Antilog amplifier

* The i/p V_i for antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} & then to base of Q_2.

$$V_{Q1\ B-E} = \frac{KT}{q} \ln\left(\frac{V_0}{R_1 I_S}\right)$$

$$V_{Q2\ B-E} = \frac{KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

Since Q_1 is tied to ground

$$V_A = -V_{Q_1 B-E} = -\frac{kT}{q} \ln\left(\frac{V_0}{R_1 I_S}\right)$$

Base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i$$

Voltage at emitter of Q_2 is

$$V_{Q2B-E} = V_B + V_{Q2E-B}$$

$$V_{Q2B-E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

But emitter voltage of Q_1 is V_A

$$V_A = V_{Q2B-E}$$

$$-\frac{kT}{q} \ln \frac{V_0}{R_1 I_S} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_S}$$

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q}\left[\ln \frac{V_0}{R_1 I_S} - \ln \frac{V_{ref}}{R_1 I_S}\right]$$

$$\frac{-q}{kT} \frac{R_{TC}}{R_2 + R_{TC}} V_i = \ln\left(\frac{V_0}{V_{ref}}\right)$$

Changing natural log ; i.e, ln to $\log_{10}$

$$[\log_{10} x = 0.4343 \ln x]$$

$$-0.4343\left(\frac{q}{KT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right)$$

$$-K'V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

$$\frac{V_o}{V_{ref}} = 10^{-K'V_i}$$

$$V_o = V_{ref}\left(10^{-K'V_i}\right)$$

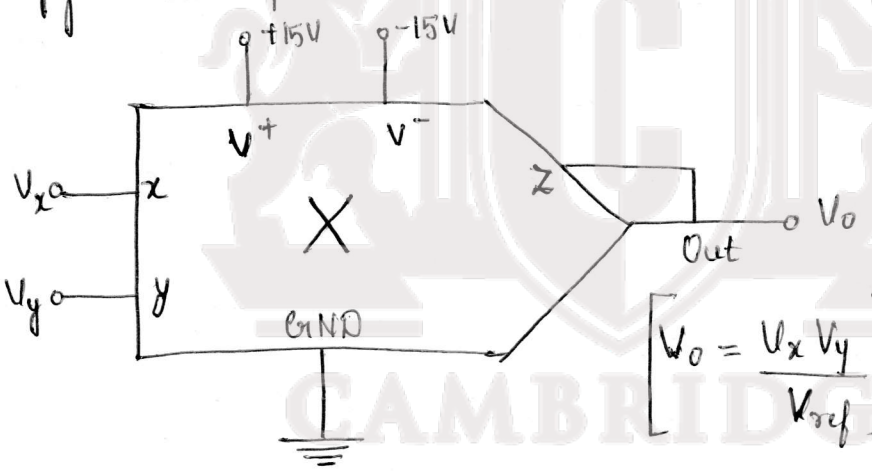
$$\left[K' = 0.4343\left(\frac{q}{KT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)\right.$$

Hence an increase of i/p by one volt causes the o/p to decrease by a decade.

ANALOG MULTIPIERS

There are number of applications of analog multipliers such as
(i) frequency doubling
(ii) measurement of real power.
(iii) detecting phase-angle difference between two signals of equal frequency.
(iv) multiplying two signals
(v) dividing one signal by another
(vi) taking square root of a signal
(vii) squaring a signal

fig(a): Multiplier Schematic Symbol.



$$\left[V_o = \frac{V_x V_y}{V_{ref}}\right]$$

In fig (a) Two signal inputs (V_x and V_y) are provided. The output is the product of the two inputs divided by a reference voltage. Thus output voltage is a scaled version of x and y inputs. The output voltage is given by

$$V_o = \frac{V_x V_y}{V_{ref}} \rightarrow (1)$$

where V_{ref} is internally set to 10 volts.

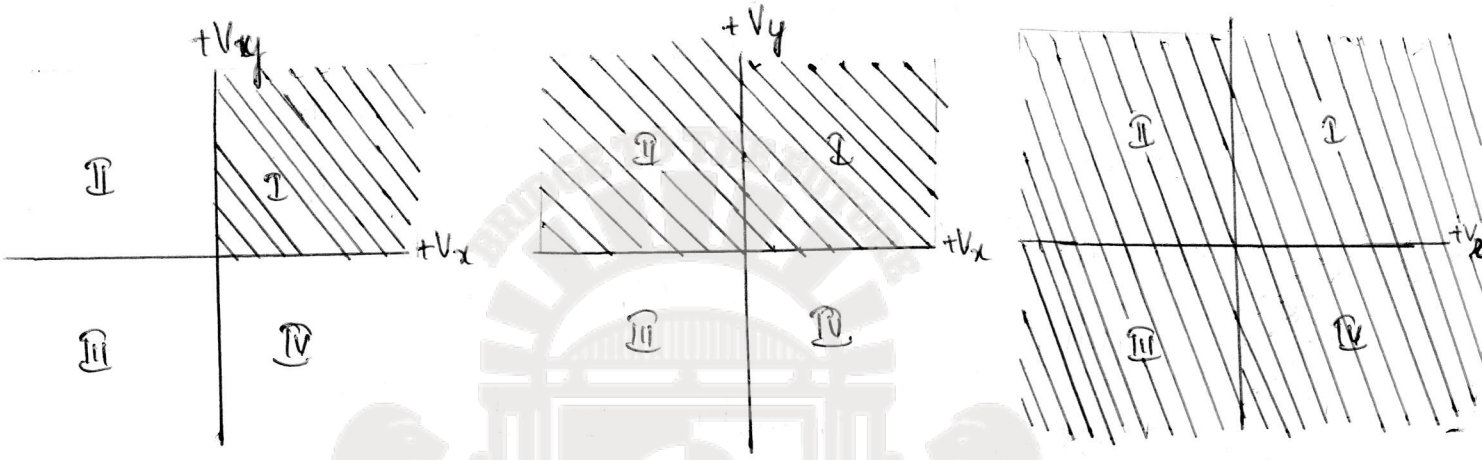
$$V_o = \frac{V_x V_y}{10}$$

as long as $V_x < V_{ref}$

$V_y < V_{ref}$

the output of the multiplier will not saturate. Power supply Voltage can range from ±8V to ±18V. Usually, multipliers are designed for the same type of power supplies as used for opamps, namely ±15V.

Cases :-



(b) One quadrant multiplier (c) Two quadrant multiplier (d) Four quadrant multiplier.

If both inputs are positive, the IC is said to be a one quadrant multiplier as shown in [fig.(b)]

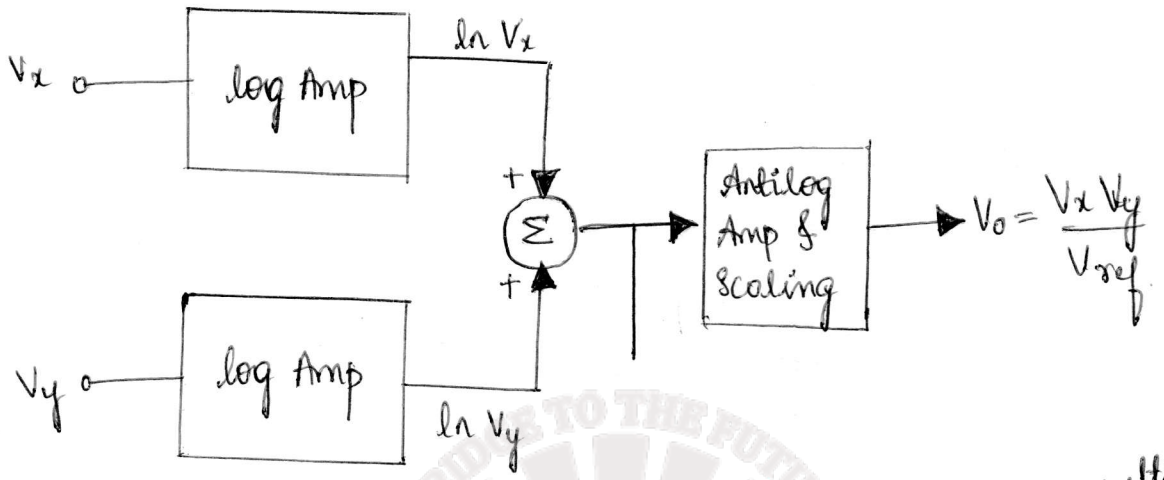
A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. [fig(c)]

If both inputs may be either positive or negative, the IC is called a four quadrant multiplier [fig(d)]

Log - Anti-log Multiplier

There can be several ways to make a circuit which will multiply according. One commonly used technique is log- antilog method. The log- antilog method relies on the mathematical relationship that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers

$$\ln V_x + \ln V_y = \ln(V_x V_y)$$



Block diagram of a log-antilog multiplier

In the above diagram, log-amps require the input and reference voltages to be of the same polarity. This restricts log-antilog multipliers to one quadrant operation. A technique that provides four quadrant multiplication is transconductance multiplier. Some of the multiplier IC chips available are AD533, AD534, AD633.

DIVIDER

Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider with input signals V_z and V_x as dividend and divisor respectively is given by

$$V_o = -V_{ref} \frac{V_z}{V_x} \rightarrow (1)$$

The result can be derived as follows. The op-amp's inverting terminal is at virtual ground Therefore,

$$I_Z = I_A$$

and

$$I_Z = \frac{V_Z}{R}$$

Output Voltage (V_A) of the multiplier is determined by the multiplication of V_x and V_y

$$V_A = \frac{V_x V_y}{V_{ref}} = \frac{V_x V_o}{V_{ref}} \longrightarrow (2)$$

Again $V_A = -I_A R$

so, $$I_A = -V_A/R = -\frac{V_x V_o}{V_{ref} R} \longrightarrow (3)a$$

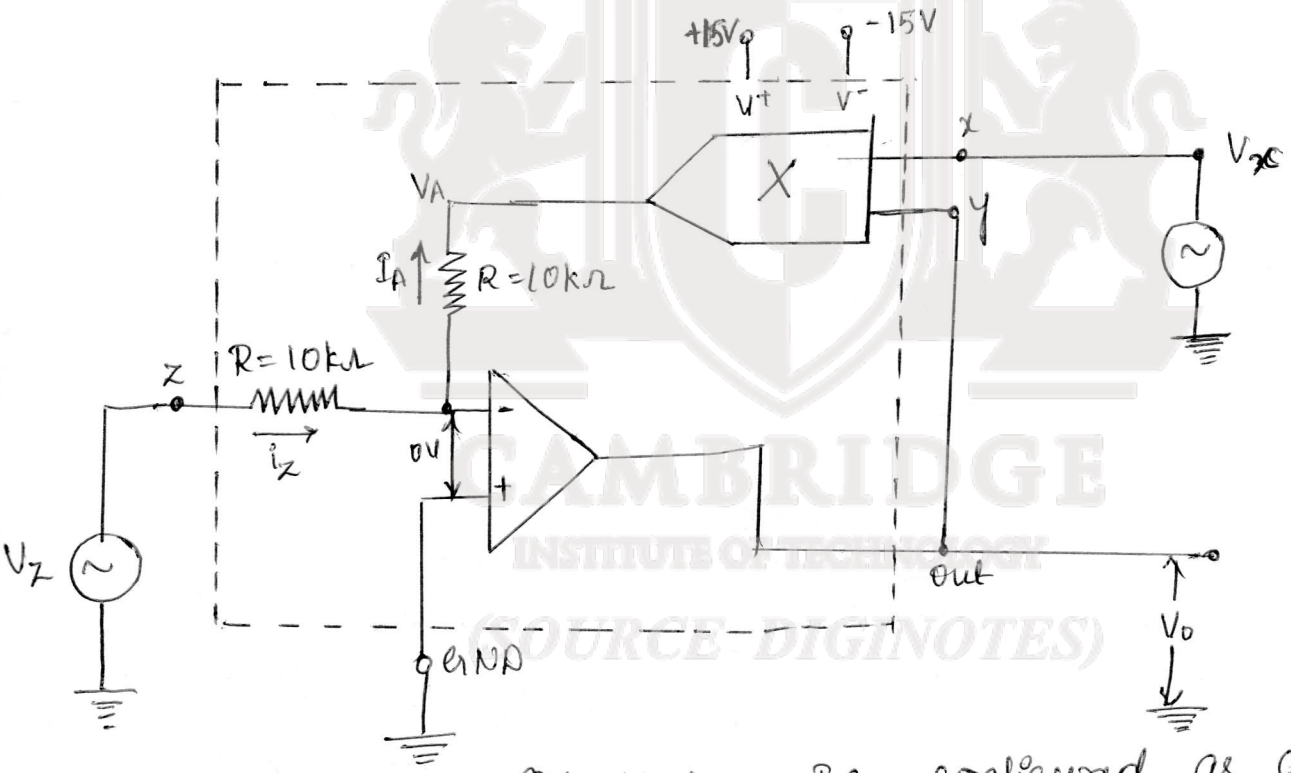


fig: Multiplier IC configured as divider

As $I_Z = I_A$

so, $$I_Z = -\frac{V_x V_o}{V_{ref} R}$$

and $$V_Z = I_Z R = -\frac{V_x V_o}{V_{ref}}$$

(Or) $V_o = -V_{ref}\frac{V_D}{V_x} \longrightarrow$ ③b

Division by zero is of course, probibited. Multiplier IC can be used for squaring a signal. Similarly, Divider circuit can be used to take the square root of a signal.

———— x ————

MODULE - 4A
ACTIVE FILTERS

~~OP-AMP NON LINEAR CIRCUITS~~

LIC → (1)

Filters: A filter is a network that allows a certain band of frequencies to pass through it and attenuates those that lie outside this band.

Depending on the pass and attenuation bands, filters can be classified into four categories.

(i) Low pass filter (LPF)
(ii) High pass filter (HPF)
(iii) Band-Pass filter (BPF)
(iv) Band-Reject filter (BRF) | Stop-Band-filter | Notch filter

The simplest way to make a filter is by using passive components (resistors, capacitors, inductors). This works well for high frequencies, ie radio frequ. However at audio frequencies, inductors become problematic, as the inductors become large, heavy and expensive.

For low frequency applications more no of turns of wire must be used which in turn adds to the series resistance degrading inductors performance ie low Q, resulting in high power dissipation.

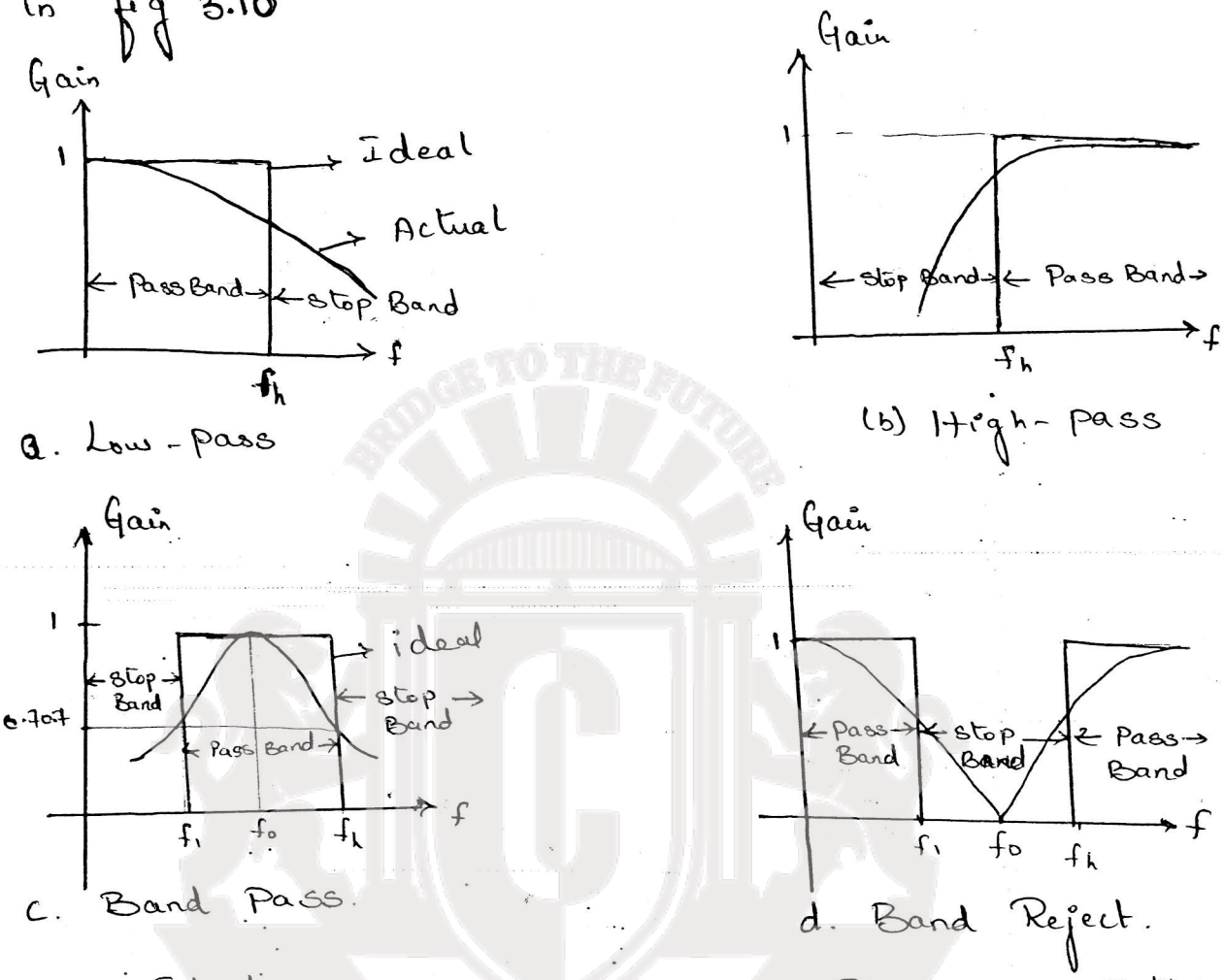
The active filters overcome the above problems of the passive filters.

The active filters use op-amp as the active element along with passive components (resistors & capacitors)

inductors are avoided

Active filters uses op-amps. Op-amps filters have the advantage that they can provide gain, thus i/p signal is not attenuated. Also op-amp is used in non-inverting configuration which offers high i/p impedance and low o/p impedance, which will help to improve the load drive capacity and the load is isolated from the frequency determining n/w.

Frequency response of filters are as shown in fig 3.10



— → Ideal

— → Practical

fig: 3.10 Frequency Response of Filters

Note: The transfer function

$$H(s) = \frac{V_o(s)}{V_i(s)} \quad \text{ie} \quad A = \frac{V_o}{V_i}.$$

Under steady state condition $s = j\omega$

$$H(j\omega) = |H(j\omega)| e^{\phi(\omega)}.$$

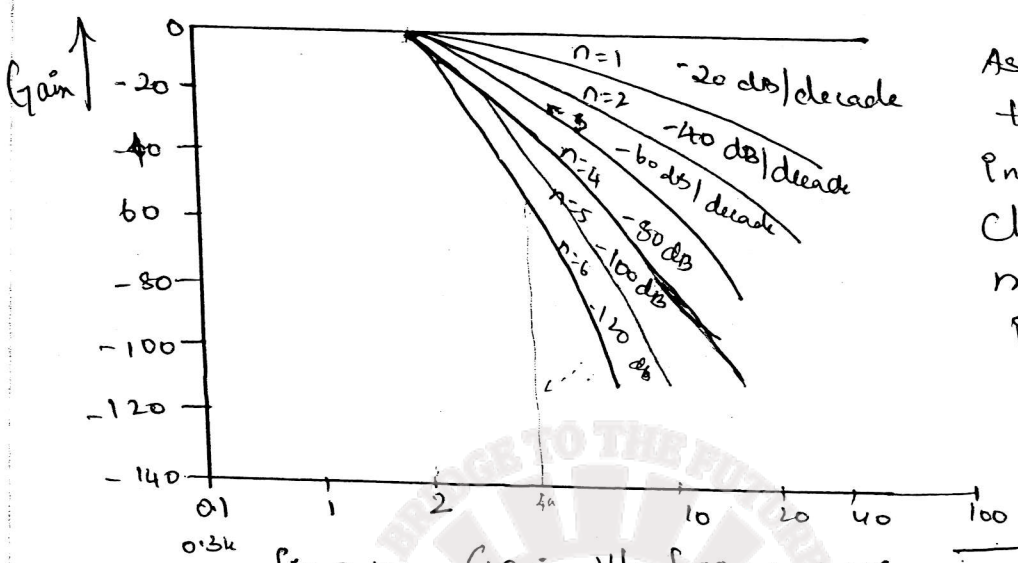
<u>Roll-off rate for different values of n</u>: Filters can also be classified based on roll off rate

If the roll of rate in the stop band (ie fall of gain with increase in frequency)

(i) $-20dB/decade$ → First order
(10 times increament in frequ)

(ii) $-40dB/decade$ → Second order

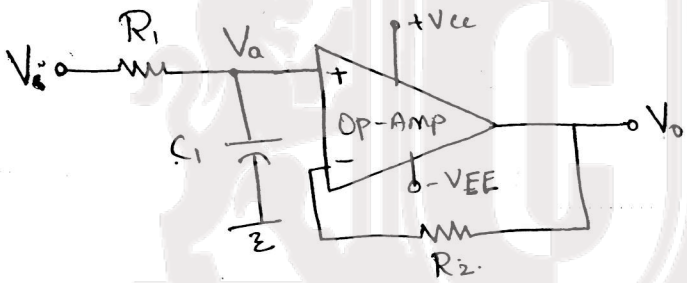
(iii) $-60dB/decade$ → Third order.



As the order of the filter increases the characteristic moves to the ideal characteristic

fig 3.11: Gain V/s frequency curve.

First order Low pass Filter: The circuit shows an first order low pass filter with an RC n/w and a Voltage follower circuit.



The resistor R_2 is included to have equalized drop at the input terminals. Thus $R_2 = R_1$.

fig: 3.12: First order Low pass filter

Since Voltage follower is used $V_o = V_a$

V_a: from fig [drop across C_1]

$$V_a = \frac{V_i \times X_{C_1}}{R_1 + X_{C_1}} = \frac{V_i \cdot \frac{1}{j\omega C_1}}{R_1 + \frac{1}{j\omega C_1}} = \frac{\frac{V_i}{j\omega C_1}}{\frac{(1 + j\omega C_1 R_1)}{j\omega C_1}}$$

$$V_a = \frac{V_i}{1 + j\omega C_1 R_1}$$

we have $V_o = V_a$

$$V_o = \frac{V_i}{1 + j\omega R_1 C_1}$$

The Voltage Gain is given by

$$A_v = \frac{V_o}{V_i} = \frac{V_i / 1 + j\omega R_1 C_1}{V_i} = \frac{1}{1 + j\omega R_1 C_1}$$

$$A_v = \frac{1}{1 + j\omega R_1 C_1}$$

Magnitude of A_v

$$|A_v| = \frac{1}{\sqrt{1 + (\omega R_1 C_1)^2}} \quad \text{ie} \quad \frac{1}{\sqrt{1^2 + \frac{1}{\omega^2 R_1^2 C_1^2}}}$$

$$|A_v| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_H}\right)^2}}$$

Let $\frac{1}{R_1 C_1} = \omega_H$

$$|A_v| = \frac{1}{\sqrt{1 + \left(\frac{\cancel{2\pi} f}{\cancel{2\pi} f_H}\right)^2}}$$

$$\boxed{|A_v| = \frac{1}{\sqrt{1 + \left(f/f_H\right)^2}}}$$

To draw the response

At $f = 0$, $A_v = \frac{1}{\sqrt{1+0}} = |A_v| = 1$

As $f \uparrow$ increases

$A_v = \downarrow$

As $f \to \infty$

$$A_v = \frac{1}{\sqrt{1+\infty}} = 1/\infty = 0$$

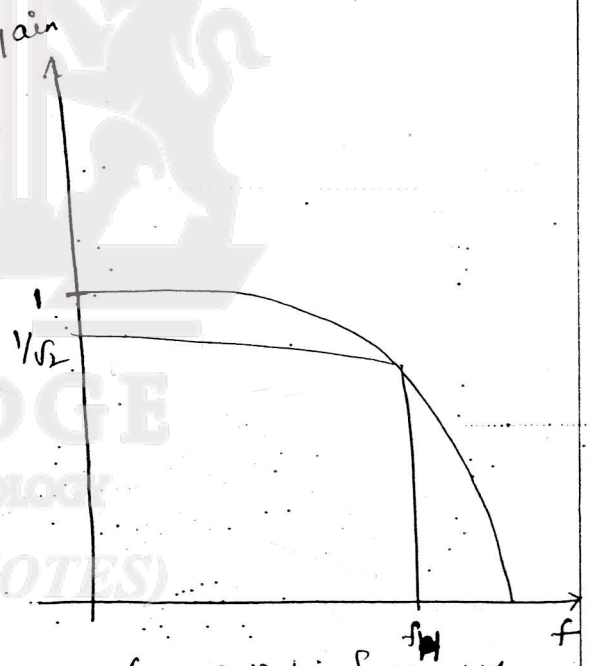


fig : 3.12.b: frequency response

at $f = f_H$

$$A_v = \frac{1}{\sqrt{1 + (f_H/f_H)}} = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}}$$ 3db down

The response shows that it is a low pass filter.

Designing : $R_1 = \frac{0.1 \times V_{BE}}{I_{B(max)}}$

$X_{C_1} = R_1$ at f_c $\quad C_1 = \frac{1}{2\pi f_c R_1}$

OP-AMP NON LINEAR CIRCUITS:

First order High pass Filter:

$R_o = R_1$ [Equalize drop]

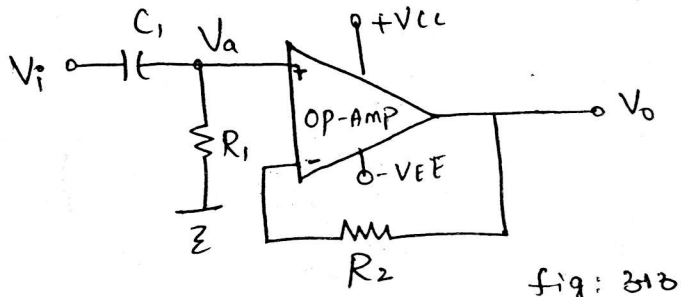


fig: 3.13 : First order High pass Filter

$$V_a = \frac{V_i \times R_1}{R_1 + \frac{1}{j\omega C_1}} = \frac{\cancel{R_1} \times V_i}{\cancel{R_1}\left(1 + \frac{1}{j\omega C_1 R_1}\right)} = \frac{V_i}{\left(1 + \frac{1}{j\omega R_1 C_1}\right)}$$

$$V_o = V_a = \frac{V_i}{1 + \frac{1}{j\omega R_1 C_1}} \longrightarrow (1)$$

$$A_v = \frac{V_o}{V_i} = \frac{\frac{\cancel{V_i}}{1 + \frac{1}{j\omega R_1 C_1}}}{\cancel{V_i}} = \frac{1}{1 + \frac{1}{j\omega R_1 C_1}}$$

Magnitude of A_v

$$|A_v| = \frac{1}{\sqrt{1 + \left(\frac{1}{\omega R_1 C_1}\right)^2}}$$

$$A_v = \frac{1}{\sqrt{1^2 + \left(\frac{1}{\omega^2 R_1^2 C_1^2}\right)}}$$

$$|A_v| = \frac{1}{\sqrt{1 + \left(\frac{\omega_L}{\omega}\right)^2}} \qquad \omega_L = \frac{1}{R_1 C_1}$$

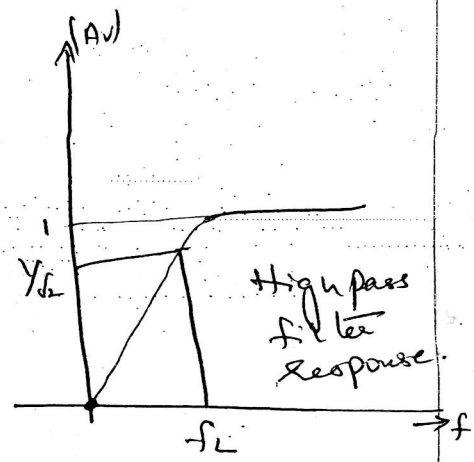
$$|A_v| = \frac{1}{\sqrt{1 + \left(\frac{2\pi f_L}{2\pi f}\right)^2}} = \frac{1}{\sqrt{1 + \left(f_L/f\right)^2}}$$

frequency response

At $f = 0$, $\frac{1}{\sqrt{1 + (f_L/0)^2}} = \frac{1}{\infty} = 0$

As $f \uparrow$ $\frac{1}{\sqrt{1 + (\text{small value})}} = A_v \uparrow$

As $f \to \infty$ $\frac{1}{1 + (f_L/\infty)} = 1$, At $f = f_L$ $A_v = \frac{1}{\sqrt{2}}$



Second order Low-pass filter

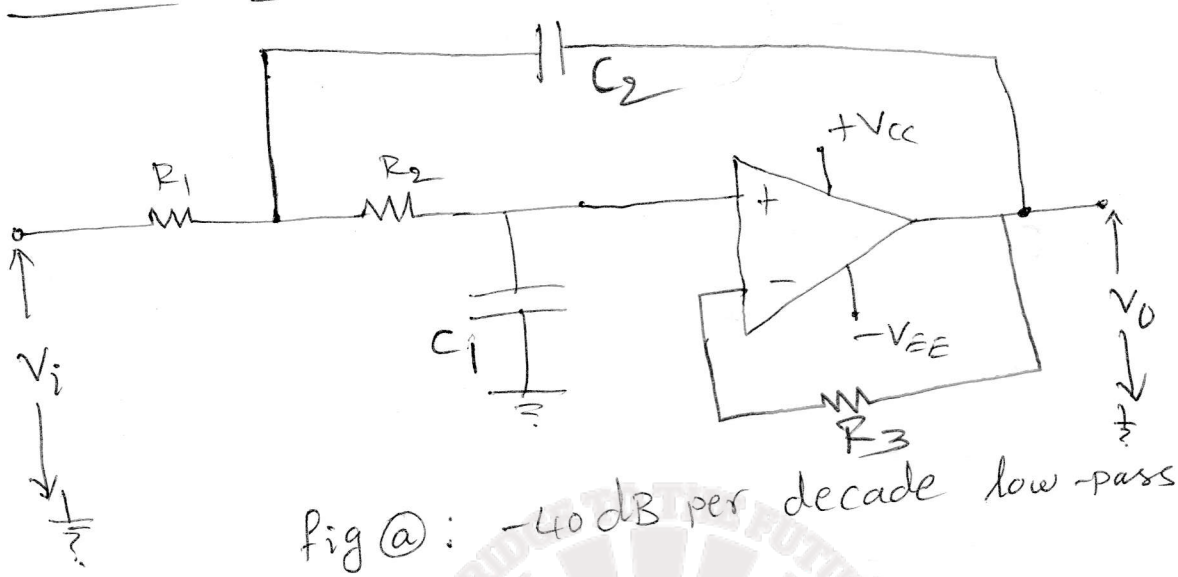


fig ⓐ : -40 dB per decade low-pass filter circuit

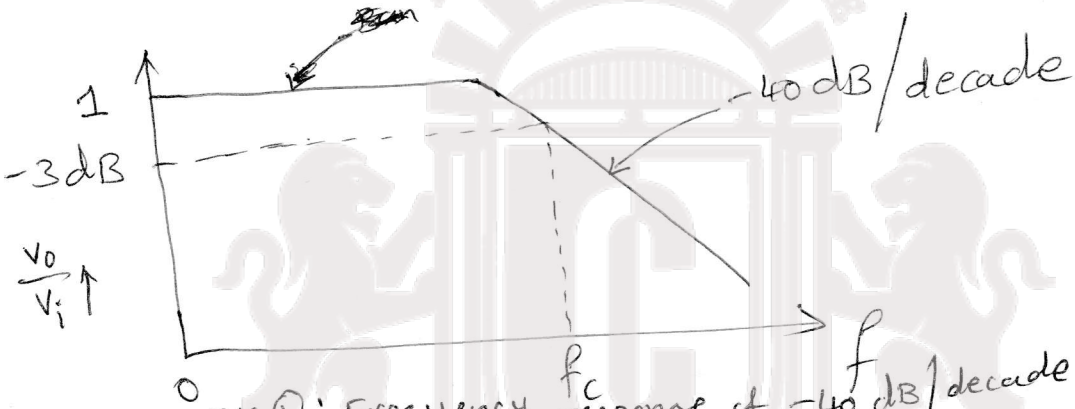


Fig ⓑ : Frequency response of -40 dB/decade low-pass filter

The basic low-pass filter (first order) has a voltage gain which falls off at the rate of -20 dB/decade.

Fig ⓐ shows a filter circuit known as a second-order low-pass filter, which has a frequency response that falls off at the rate of -40 dB/decade above the upper cut-off frequency. This steeper roll-off rate is achieved by using the C_1R_2 section together with feedback from the output via capacitor C_2 to the junction of R_1 and R_2.

Design:

A simple approach can be taken in the design of a -40 dB/decade low pass filter.

The resistance of $R_1 + R_2$ is first determined in the usual way. i.e, $R_1 + R_2 = \frac{0.1 V_{BE}}{I_{B\,max}}$

Then, $R_1 = R_2 = \frac{R_1 + R_2}{2}$

The capacitor C_1 is calculated from

$$X_{C_1} = \sqrt{2}\, R_2 \text{ at } f_c$$

and

$$C_2 = 2C_1$$

to give

$$R_1 = \sqrt{2}\, X_{C_2} \text{ at } f_c$$

Design a second-order low-pass filter circuit to have a cutoff frequency of 1 KHZ

Solution:

The frequency response of the 741 extends to approximately 800 KHZ when its voltage gain is 1, so the 741 op-amp is suitable.

$$\therefore R_1 + R_2 = \frac{0.1 V_{BE}}{I_{B\,max}} = \frac{0.1 \times 0.7}{500 \times 10^{-9}} = 140 K\Omega$$

$$R_1 = R_2 = \frac{R_1 + R_2}{2} = \frac{140 K\Omega}{2} = 70 K\Omega$$

(use 68 KΩ standard value)

$$R_3 \simeq R_1 + R_2 = 70 K\Omega + 70 K\Omega$$

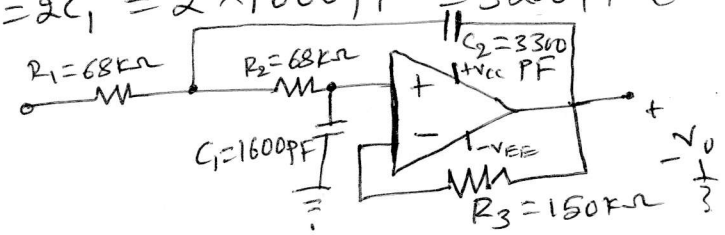
$$R_3 \simeq 140 K\Omega \text{ (use 150 KΩ standard value)}$$

$$X_{C_1} = \sqrt{2}\, R_2 \text{ at } f_c$$

$$C_1 = \frac{1}{2\pi f_c \sqrt{2}\, R_2} = \frac{1}{2\pi \times 1 KHz \times \sqrt{2} \times 68 K\Omega}$$

$C_1 = 1655$ PF (use 1600 pF standard value)

$C_2 = 2C_1 = 2 \times 1600$ pF $= 3200$ pF (use 3300 pF standard value)



problem on ~~LPF~~ 1st order LPF

Using a 741 op-amp, design a first-order active LPF to have a cut-off frequency of 1 KHz.

Solution:

$$R_1 = \frac{0.1\, V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7}{500\,nA}$$

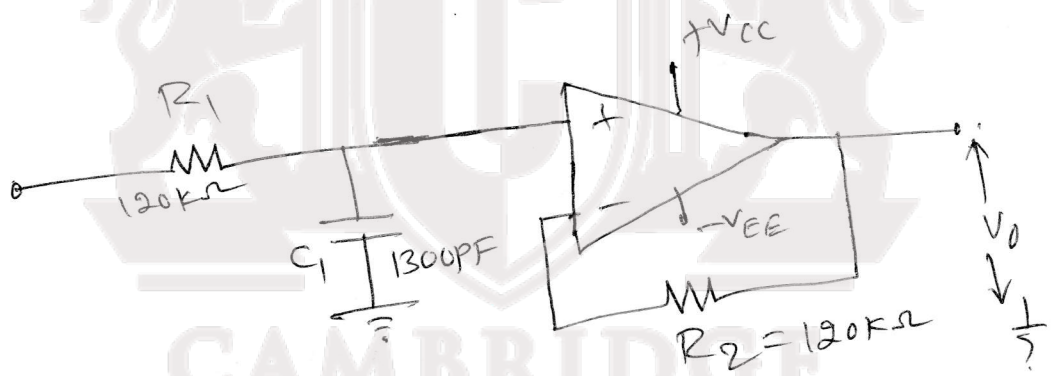
$R_1 = 140\,k\Omega$ (use $120\,k\Omega$ standard value)

$R_2 = R_1 = 120\,k\Omega$

$X_{C_1} = R_1$ at f_c

$$\therefore C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 1\,KHz \times 120\,k\Omega}$$

$C_1 = 1326\,pF$ (use 1300 pF standard value)



problem on 1st order HPF

Design a first order high-pass filter to have a cut-off frequency of 5KHz. Use LM108 op-amp and estimate the highest frequency that can be passed.

Solution:

Because the LM108 has an extremely low input bias current, it should be treated as a BIFET op-amp. Therefore, select a capacitance value for C_1 very much larger than stray capacitance.

Let $C_1 = 1000\,pF$

$$R_1 = \frac{1}{2\pi f_c C_1} = \frac{1}{2\pi \times 5\,kHz \times 1000\,pF}$$

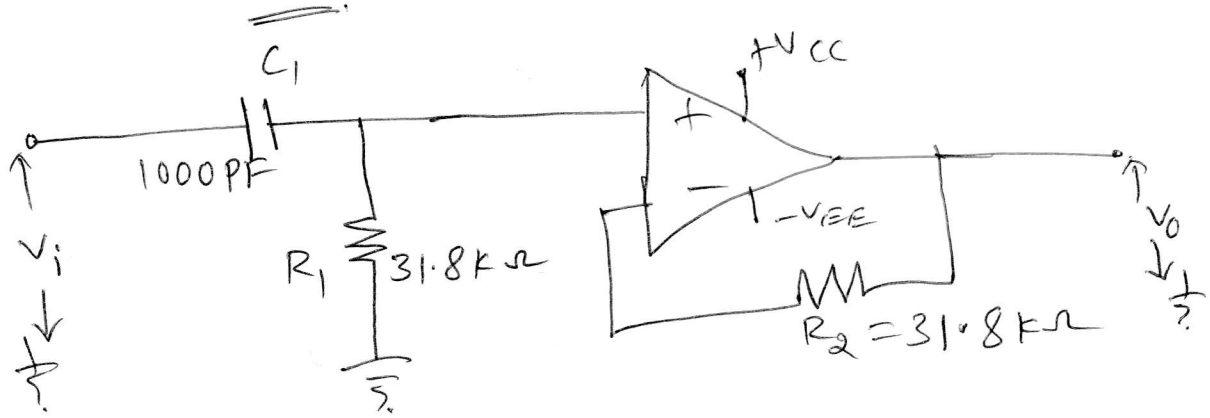
$$= 31.8\,k\Omega$$

$$R_2 = R_1 = 31.8\,k\Omega$$

From the LM108 gain/frequency response, the op-amp unity gain frequency is $f_u \simeq 1\,MHz$.

$$f_2 = \frac{f_u}{A_v}$$

$$= 1\,MHz$$



Second-order High-pass filter

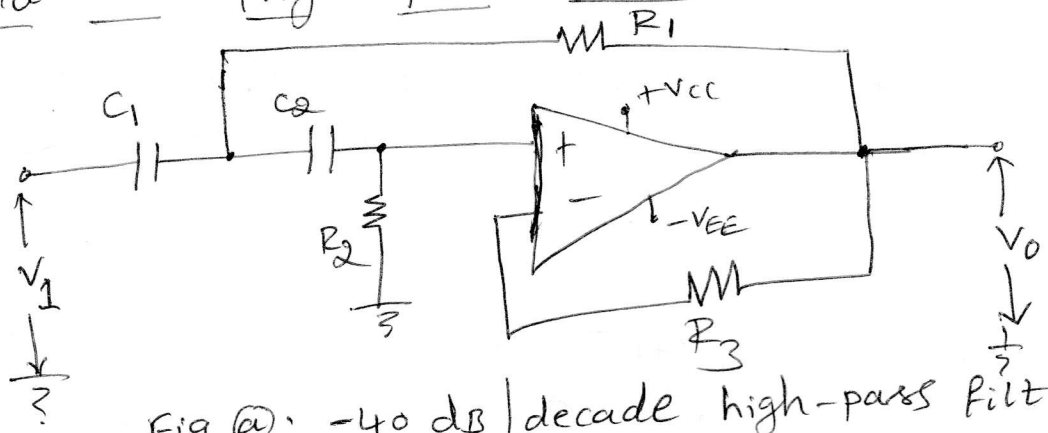


Fig ⓐ: −40 dB/decade high-pass filter circuit

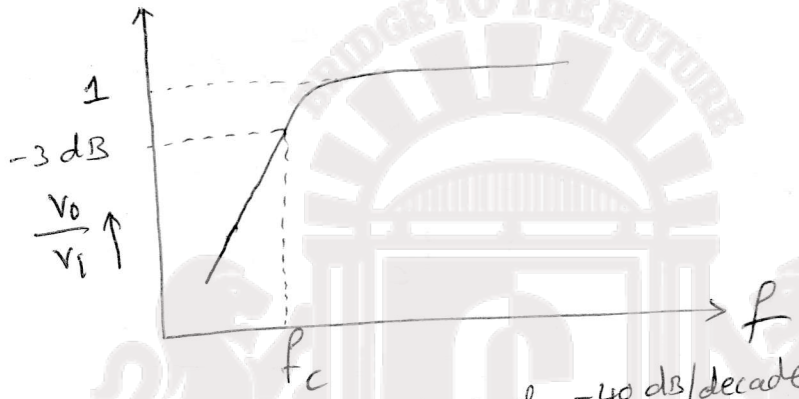


Fig ⓑ: Frequency response of −40 dB/decade High-pass filter.

The second-order (−40 dB/decade) high-pass filter circuit is similar to the low-pass filter (second order) except that the resistor and capacitor positions are interchanged.

$$R_2 = \frac{0.1 V_{BE}}{I_{B,max}}$$

Capacitor C_2 is selected to give

$$R_2 = \sqrt{2}\, X_{C_2} \text{ at } f_c$$

then $C_1 = C_2$

and $R_1 = R_2/2$

to give $X_{C_1} = \sqrt{2}\, R_1$ at f_c

Design a second-order high-pass active filter to have a cutoff frequency of 12 KHz. Use a 715 op-amp and estimate the highest signal frequency that will be passed.

Solution:

From the 715 data sheet

$I_{B(max)} = 1.5\ \mu A$

$$R_2 = \frac{0.1\ V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7}{1.5\ \mu A} = 47\ k\Omega$$

$R_1 = R_2/2 = 23.5\ k\Omega$ Use (22 kΩ and 1.5 kΩ in series)

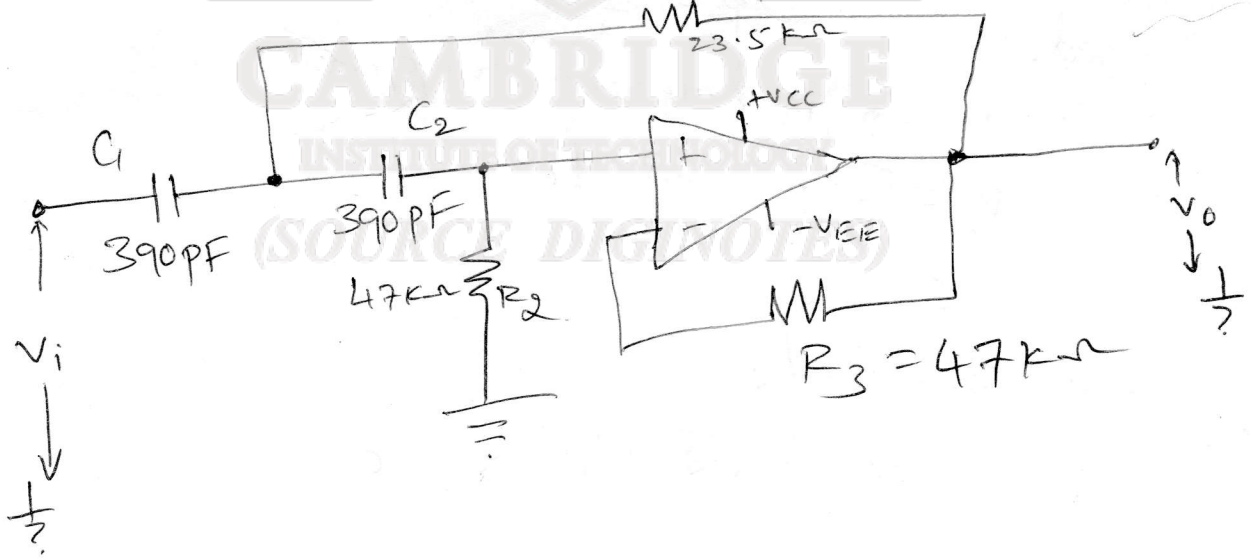
$R_3 = R_2 = 47\ k\Omega$

$R_2 = \sqrt{2}\ X_{C_2}$ at f_c

$$\therefore C_2 = \frac{1}{2\pi f_c (R_2/\sqrt{2})} = \frac{\sqrt{2}}{2\pi \times 12\ KHz \times 47\ k\Omega}$$

$\therefore C_2 = 398\ pF$ (Use 390 pF standard value)

$C_1 = C_2 = 390\ pF$



Solution

From the 741 data sheet in Appendix 1-1 (enlarged frequency response in Fig. 5-13(a)), the op-amp unity gain cutoff frequency is $f_u \approx 800$ kHz. From Eq. 5-6, the high cutoff frequency of each op-amp is

$$f = \frac{f_u}{A_v}$$

$$\approx 800 \text{ kHz}$$

From Eq. 11-12, the circuit upper cutoff frequency is approximately,

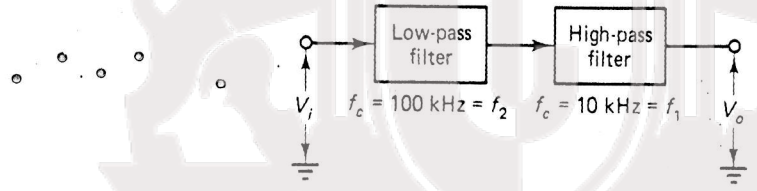
$$f_c = 0.65f = 0.65 \times 800 \text{ kHz}$$

$$= 520 \text{ kHz}$$

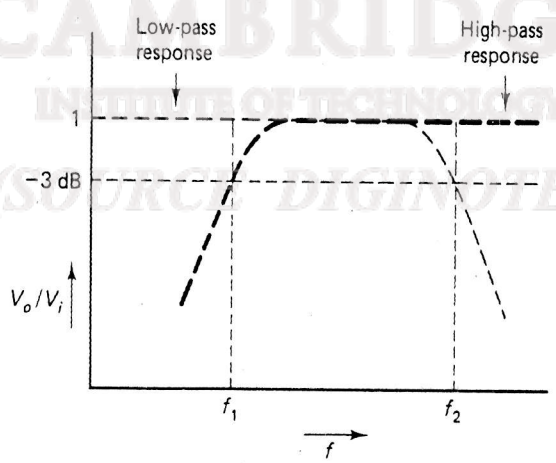
11-8 BANDPASS FILTERS

Multi-stage Bandpass Filter

A bandpass filter can be constructed simply by connecting low-pass and high-pass filters in cascade (see Fig. 11-14). For example, suppose a low-pass circuit with $f_c = 100$ kHz is cascaded with a high-pass circuit which has $f_c = 10$ kHz. The low-



(a) Cascaded low-pass and high-pass filters



(b) Bandpass frequency response

Figure 11-14 Bandpass filter circuit consisting of low-pass and high-pass stages connected in cascade. The low-pass stage sets the high cutoff frequency f_2 and the high pass stage determines the low cutoff frequency f_1.

pass circuit will pass all frequencies up to 100 kHz, while the high-pass circuit will block all frequencies below 10 kHz. So, the combination gives a filter with a pass band from 10 kHz to 100 kHz.

Single-Stage First-Order Bandpass Filter

A single-stage bandpass filter is shown in Fig. 11-15. If the capacitors were not present, the circuit would look like an inverting amplifier. The capacitors are selected to have X_{C2} large enough to be neglected at low frequencies and X_{C1} small enough to be neglected at high frequencies.

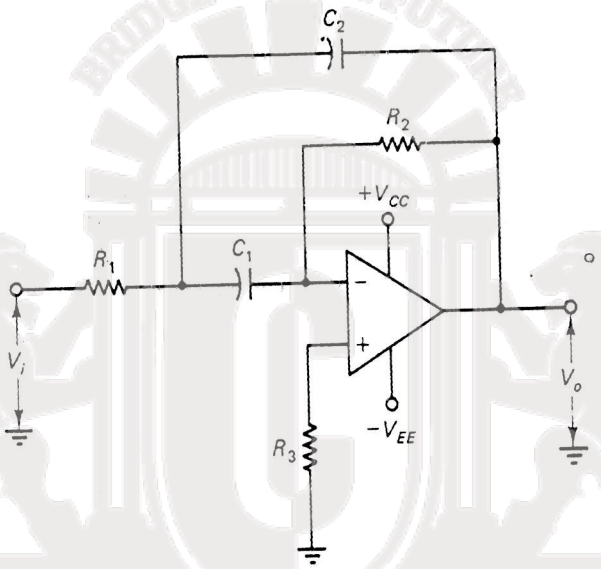


Figure 11-15 Single-stage bandpass filter circuit. For a wide pass band, the cutoff frequencies are set by making $X_{C1} = R_1$ at f_1 and at $X_{C2} = R_2$ at f_2.

At low frequencies, X_{C2} is so large that it can be eliminated from the low frequency equivalent circuit. As shown in Fig. 11-16(a), the circuit is an inverting amplifier with a voltage gain of

$$A_v = \frac{R_2}{Z_1} = \frac{R_2}{\sqrt{(R_1^2 + X_{C1}^2)}}$$

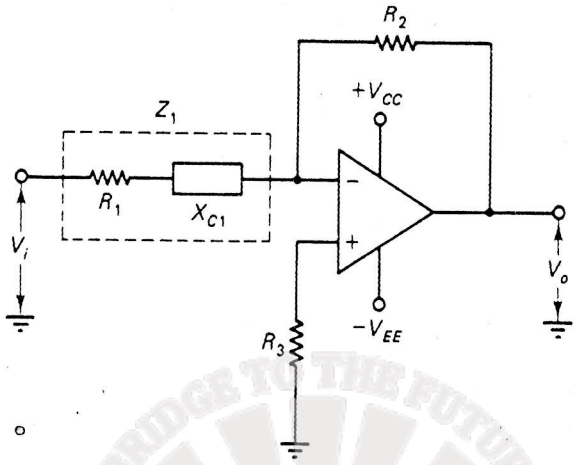
At signal frequencies in the pass band of the circuit, X_{C1} becomes much smaller than R_1, So, the circuit gain becomes

$$A_v \approx \frac{R_2}{R_1}$$

The above equations show that for voltage gain to be down by 3 dB (from the mid-frequency gain),

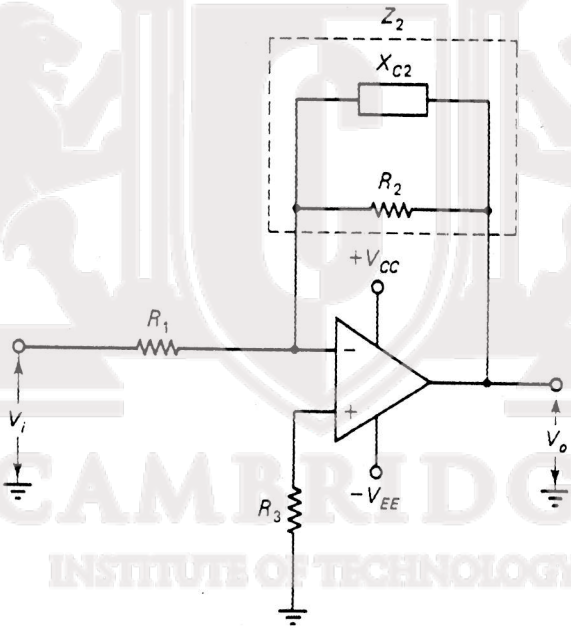
$$X_{C1} = R_1 \text{ at } f_1 \tag{11-16}$$

where f_1 is the low cutoff frequency.



(a) Low frequency equivalent circuit

$$A_v = \frac{R_2}{Z_1}$$



(b) High frequency equivalent circuit

$$A_v = \frac{Z_2}{R_1}$$

Figure 11-16 Low frequency and high frequency equivalent circuits for the single-stage bandpass filter. Capacitor C_2 can be neglected at low frequency and C_1 can be disregarded at high frequency.

At high frequencies, X_{C1} becomes so small compared to R_1 that it can be eliminated from the high-frequency equivalent circuit. But, X_{C2} is no longer large enough to be ignored. So, the high frequency equivalent circuit is as shown in Fig. 11-16(b). Once again, the circuit is an inverting amplifier and its voltage gain is

$$A_v = \frac{X_{C2} \parallel R_2}{R_1} = \frac{1}{R_1\sqrt{[(1/R_2)^2 + (1/X_{C2})^2]}}$$

At frequencies in the pass-band, X_{C2} is much larger than R_1. So, the circuit voltage gain is once again

$$A_v \approx \frac{R_2}{R_1}$$

From the above equations, the voltage gain is down by 3 dB from its mid-frequency value when,

$$X_{C2} = R_2 \text{ at } f_2 \tag{11-17}$$

where f_2 is the high cutoff frequency.

It is seen that the circuit behaves as an inverting amplifier when the signal frequency is in the pass band, as a high-pass filter for low frequencies, and as a low-pass filter for high frequencies. The low cutoff frequency is determined by Eq. 11-15 and the high cutoff frequency is calculated from Eq. 11-17.

The normal design approach of selecting the resistors first is likely to give unacceptably small capacitance values whether bipolar or BIFET op-amps are used. So, it is usually best to commence by selecting the value of the smallest capacitor (C_2). Then R_2 can be determined from Eq. 11-17 and R_1 can be calculated in relation to R_2 for the desired voltage gain. The value of R_1 can be substituted into Eq. 11-15 to calculate C_1. Since direct current through R_1 is interrupted by C_1, resistor R_3 should be made equal to R_2 for resistance equality at the op-amp input terminals.

Example 11-9

Design a single-stage bandpass filter, as in Fig. 11-15, to have a voltage gain of 1 and a pass band from 300 Hz to 30 kHz.

Solution

Select $C_2 = 1000$ pF

From Eq. 11-17, $X_{C2} = R_2$ at f_2

or, $$R_2 = \frac{1}{2\pi f_2 C_2} = \frac{1}{2\pi \times 30 \text{ kHz} \times 1000 \text{ pF}}$$

$= 5.3$ kΩ (use 5.36 kΩ ±1% standard value)

$R_3 \approx R_2 = 5.36$ kΩ (use 5.6 kΩ standard value)

For $A_v = 1$ $R_1 = R_2 = 5.36$ kΩ

From Eq. 11-16 $$C_1 = \frac{1}{2\pi f_1 R_1} = \frac{1}{2\pi \times 300 \text{ Hz} \times 5.36 \text{ k}\Omega}$$

$= 0.1$ μF (standard value)

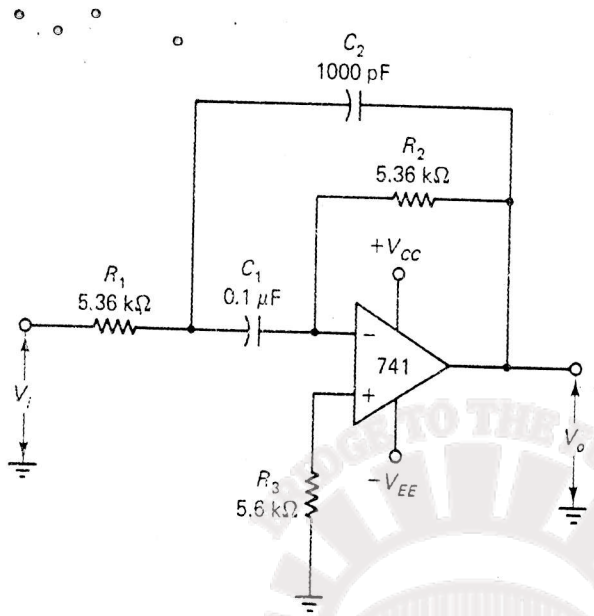


Figure 11-17 Bandpass filter designed in Example 11-9; f_1 = 300 Hz and f_2 = 30 kHz.

Wide-Band and Narrow-Band Bandpass Filters

The bandpass filter discussed above is essentially a wide-band circuit, and its typical frequency response is illustrated in Fig. 11-18(a). Narrow-band bandpass filters have the kind of frequency response shown in Fig. 11-18(b).

The bandwidth of the filter circuit is,

$$B = f_2 - f_1 \tag{11-18}$$

The circuit *Q factor* is the relationship of the center frequency f_o to the bandwidth.

$$Q = \frac{f_o}{B} \tag{11-19}$$

The Q factor is a *figure of merit* for a filter circuit. It defines the selectivity of the filter in passing the center frequency and rejecting other frequencies. Figure 11-18(b) shows that a filter with a Q of 10 has a much narrower bandwidth than a filter with Q equal to 1. The filter with the higher Q is the most selective of the two. Narrow-band filters are usually classified as those with a Q factor greater than 5, while wide-band circuits have a Q less than 5.

The center frequency of the filter can be determined from,

$$f_o = \sqrt{(f_1 f_2)} \tag{11-20}$$

For the wideband filter designed in Example 11-9,

$$f_o = \sqrt{(f_1 f_2)} = \sqrt{(300 \text{ Hz} \times 30 \text{ kHz})}$$
$$= 3 \text{ kHz}$$

Solution

Select $C_1 = C_2 = 1000$ pF

From Eq. 11-20, $f_0 = \sqrt{(f_1 f_2)} = \sqrt{(10.3 \text{ kHz} \times 10.9 \text{ kHz})}$

$= 10.6$ kHz

From Eq. 11-24, $R_5 = R_6 = \dfrac{1}{2\pi C_1 f_o} = \dfrac{1}{2\pi \times 1000 \text{ pF} \times 10.6 \text{ kHz}}$

$= 15.01$ kΩ (use 15 kΩ standard value)

$R_1 = R_3 = R_4 = R_7 = R_8 \approx R_5 = 15$ kΩ

From Eqs. 11-18 and 11-19, $Q = \dfrac{f_o}{f_2 - f_1} = \dfrac{10.6 \text{ kHz}}{10.9 \text{ kHz} - 10.3 \text{ kHz}}$

$= 17.7$

Eq. 11-26, $R_2 = R_1(2Q - 1) = 15 \text{ k}\Omega[(2 \times 17.7) - 1]$

$= 515$ kΩ (use 511 kΩ ±1%)

11-10 BANDSTOP FILTER

The function of a *bandstop filter*, also known as a *band-reject filter*, is to block a band of signal frequencies. This is the inverse of the bandpass filter function. A bandstop filter with a very narrow stop band is sometimes known as a *notch* filter.

Low-Pass and High-Pass Filters as Bandstop Filter

Figure 11-21(a) shows how a bandstop filter can be constructed by parallel-connecting a low-pass filter and a high-pass filter. The circuit inputs can be connected in

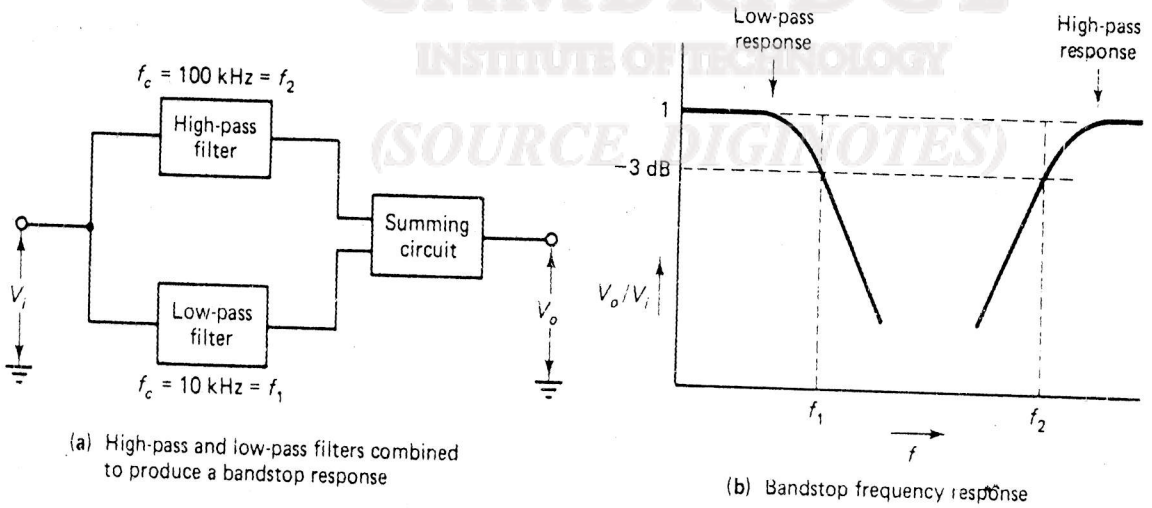


Figure 11-21 Bandstop filter consisting of parallel-connected low-pass and high-pass circuits with a summing circuit to combine their outputs. The high-pass stage determines f_2, and the low-pass stage sets f_1.

parallel without any problem, but the outputs must be applied to a summing circuit, as illustrated, to avoid one output overloading the other. Suppose that the low-pass circuit has a cutoff frequency of 10 kHz and that the cutoff frequency of the high-pass circuit is 100 kHz. The low-pass circuit will block signal frequencies above 10 kHz, while the high-pass circuit will block frequencies below 100 kHz. The result is a stop band of 10 kHz to 100 kHz, as illustrated in Fig. 11-21(b).

Note that the frequency limits of the stop band are those frequencies at which the signal is −3 dB from its normal output level. The low-pass and high-pass filters can be first-order, second-order, or higher, for any desired fall-off rate of the bandstop frequency response.

Bandpass and Summing Circuit as Bandstop

Another method of creating a bandstop filter is to sum the output of a bandpass filter with its own input signal, as illustrated in Fig. 11-22(a). In this case, the bandpass filter must have a voltage gain of −1, that is, its output must be the inverse of the input signal. Alternatively, the signal might be amplified to the same level as the bandpass output and inverted if necesary.

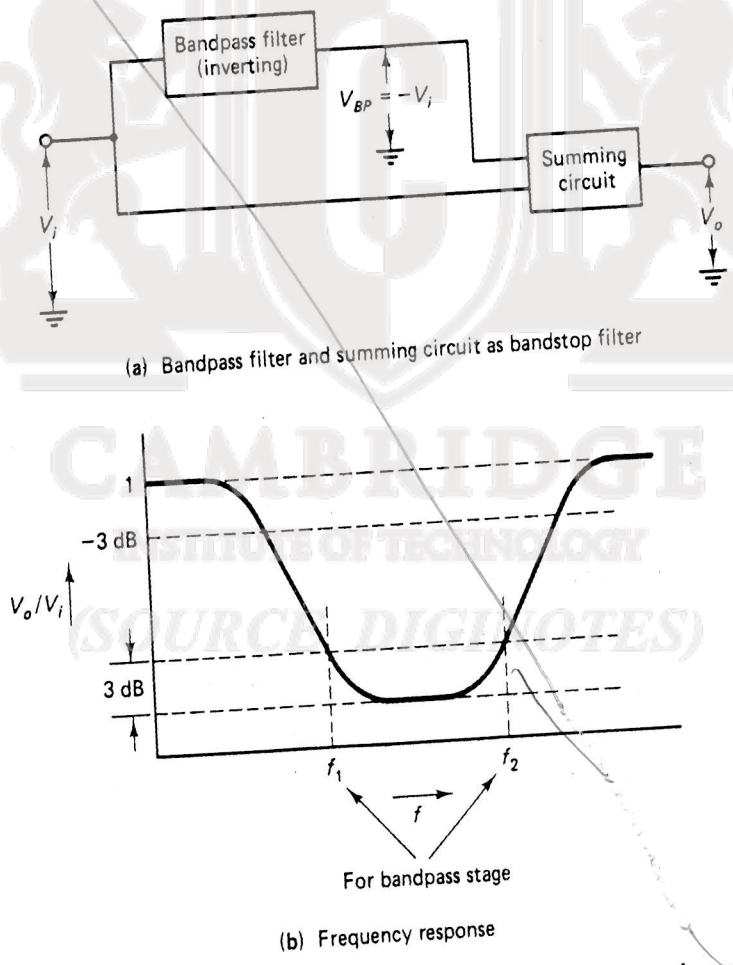


Figure 11-22 Bandstop filter made up of a bandpass stage and a summing circuit. The output is 3 dB above the attenuated level at the cutoff frequencies of the bandpass circuit.

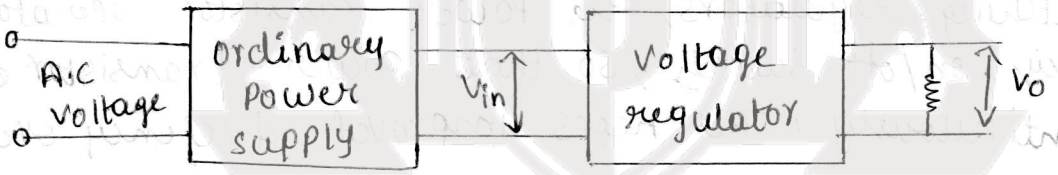
VOLTAGE REGULATORS

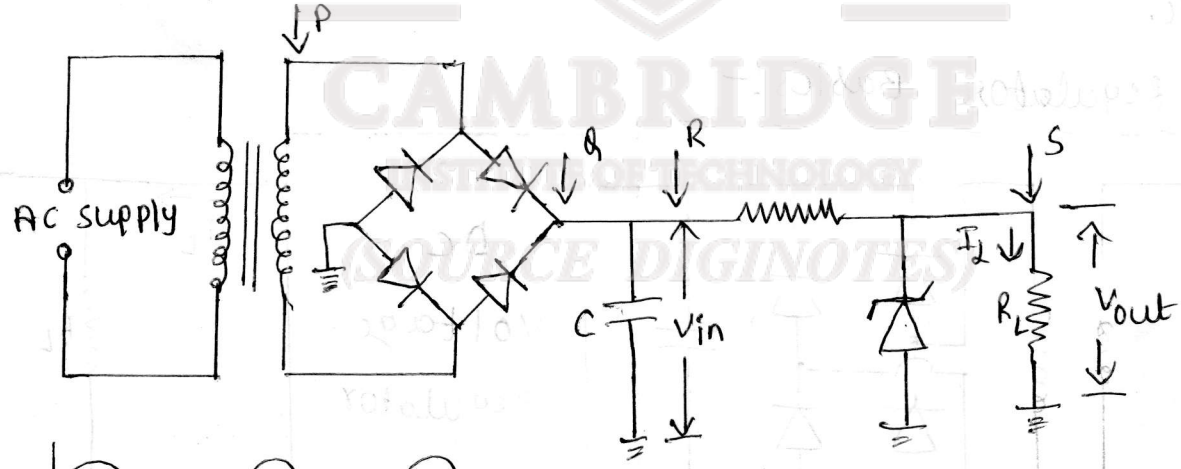
Introduction:-

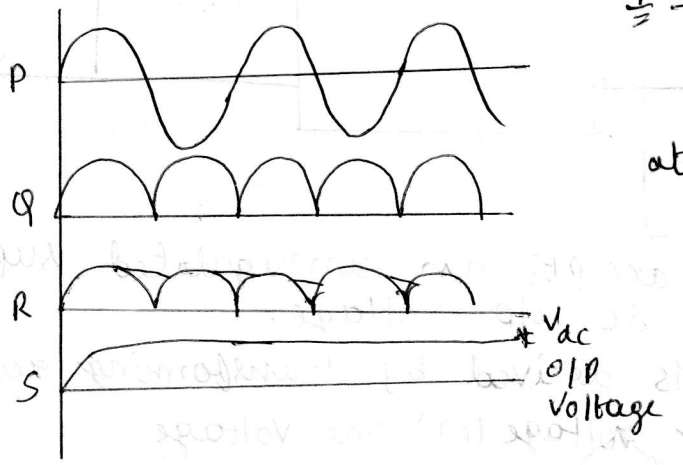
The dc voltage required by electronic circuit is normally derived by transforming, rectifying and smoothing the standard domestic (or) industrial ac supply. The dc voltage so obtained is not sufficiently stable and thus cannot be used for many applications, These dc voltages have large ripples to an unacceptable level.

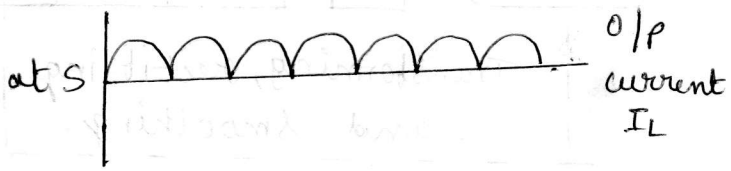
A voltage regulator is used to provide a stable dc voltage for powering electronic circuit. A voltage regulator not only should provide a stable dc voltage but also should provide a substantial o/p current.

The voltage regulator is used to provide a stable d.c voltage & to attenuate ripple as shown.









All voltage regulators employ zener diode as a stable reference voltage source. If large load current is to be driven by the load then transistors are employed. When an error amplifier is employed a vast improvement in the voltage regulator can be acheived. IC op-amps are ideal error amplifiers.

IC op-amps are classified as:

(i) Series voltage regulators

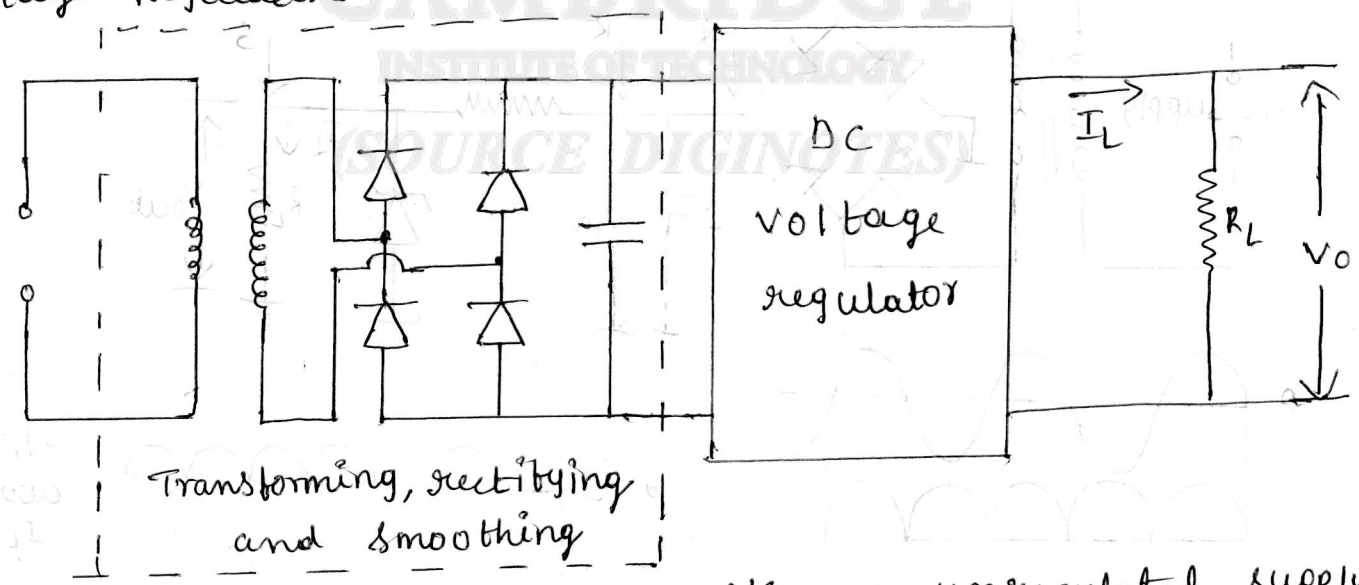
(ii) Switching regulators

Series voltage regulators:-

Uses a power transistor known as pass transistor connected in series b/w the unregulated dc i/p & the load. The o/p is controlled by the continuous voltage drop across the series pass transistor. Since transistor operators in active low linear regions the regulators may have fixed (or) variable o/p voltage & can be +ve or -ve.

In switching regulators, the power transistor operators as a high frequency on/off switch, so that power transistor doesn't conduct continuously. This keeps improved efficiency over series regulator.

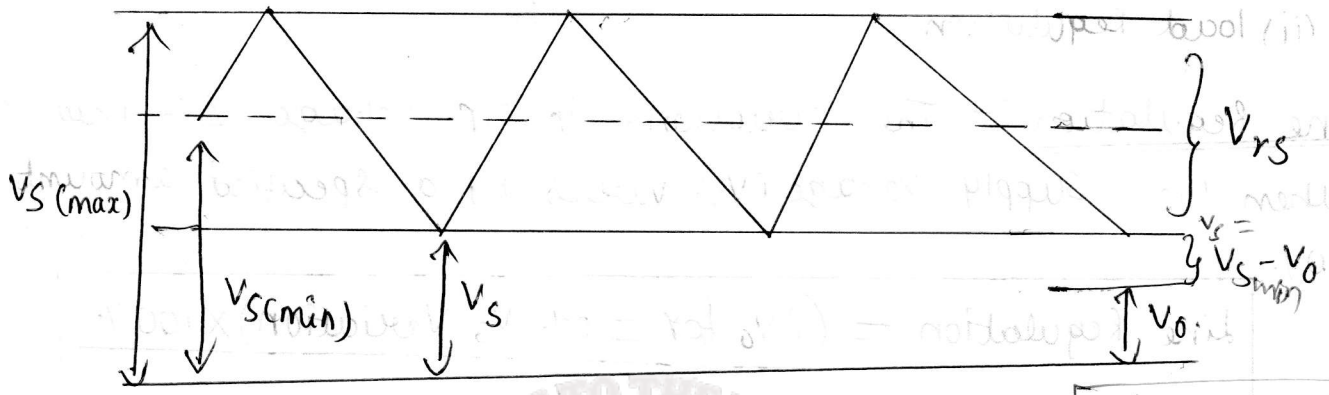
Voltage Regulator Basics:-



An dc voltage regulator accepts an unregulated supply voltage and provides a stable dc o/p voltage.

The unregulated supply is derived by transforming, rectifying and smoothing an ac supply voltage (or) line voltage.

A voltage regulator will produce a stable o/p voltage regardless of variations in line voltage (or) load current



Regulated i/p and o/p voltage $\boxed{V_0 = V_s - 2V}$ or $\boxed{V_0 = V_s - 3V}$

where :-

V_S → Regulator supply voltage

V_0 → o/p voltage

V_{rs} → ripple voltage, which is super imposed on the average dc voltage.

The peak to peak amplitude of the ripple voltage depends on the level of load current becoming greater than the highest load current, and smallest when the load current falls to zero.

There is usually some o/p voltage ripple (V_{ro}), but this is normally very much smaller than that of supply voltage ripple.

The o/p voltage provided by the voltage regulator is normally atleast 2V lower than $V_{S(min)}$.

Regulator Performance:-

The o/p voltage of a regulator is perfectly constant independent of

(i) variation in line supply

(ii) variation in load current

(iii) variation in temperature.

Practically voltage regulators do have some o/p ripple, and the o/p voltage is affected by variations in load current & line voltage.

The performance of the voltage regulator is defined in terms of

(i) line Regulation (iii) Ripple Rejection

(ii) load Regulation

Line Regulation :- The variations in o/p voltage ΔV_o that occurs when the supply voltage (V_s) varies by a specified amount usually 10%.

$$\text{Line Regulation} = \frac{(\Delta V_o \text{ for } \pm 10\% \ V_s \text{ Variation}) \times 100\%}{V_o}$$

Load Regulation :-

The variation in o/p voltage, ΔV_o due to the variations in load current variations

$$\text{Load Regulation} = \frac{(\Delta V_o \text{ for } \Delta I_L = I_L \max) \times 100\%}{V_o}$$

Ripple Rejection :-

It is measure of how much the voltage regulator attenuates the supply voltage ripple. unit is decibels.

$V_{rs} \rightarrow$ Supply ripple voltage

$V_{ro} \rightarrow$ Output ripple voltage.

$$\text{Ripple Rejection} = 20 \log\left(\frac{V_{rs}}{V_{ro}}\right) db$$

Series op-amp regulators :-

Figure shows a regulator using discrete components The circuit consists of 4 parts :

1. Reference Voltage circuit
2. Error amplifier
3. Series pass transistor
4. Feedback n/w

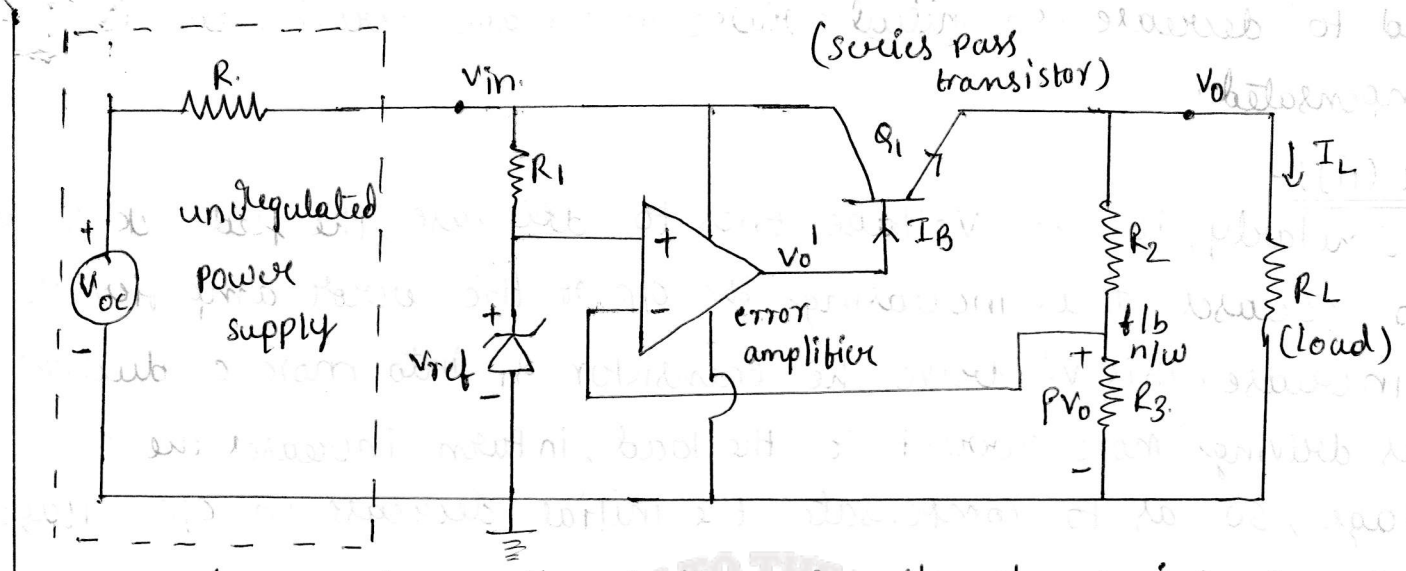


Figure above shows the circuit of series op-amp regulator. It employs principle of feedback to hold the output voltage constant despite changes in line voltage & load current. The transistor Q_1 is called pass transistor because all the load current passes through it. The sample and adjust circuit is the voltage divider that consists of R_3 & R_2. The voltage divider samples the o/p voltage and delivers the sampled o/p to the inverting terminal of the error amplifier. The sampled o/p is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The o/p V_o' of the error amplifier drives the series pass transistor. [The series pass transistor is in series with unregulated dc voltage V_{in} & the regulated o/p voltage V_o]

Operation :-

The unregulated dc supply is fed to the voltage regulator, and it gives a constant & stable voltage (because it will absorb the diff b/w the two).

Case (i) :-

Suppose the o/p voltage increases due to any reason, This causes an increase across R_3 i.e feedback o/p βV_o. Thus resulting in reduction in V_o' (error amplifier o/p). Thus base voltage of Q_1 decreases thus driving the transistor Q_1 into less conduction, & thus drives less current into the load causing voltage across

load to decrease. so initial raise in voltage across load is compensated.

Case (ii):-

Similarly, if the voltage tries to decrease, the feedback voltage also decreases. Thus increasing the o/p of the error amplifier V_o' to increase. This V_o' drive the transistor Q_1 into more conduction, thus driving more current to the load, in turn increases the o/p voltage, so as to compensate the initial decrease in o/p voltage.

The o/p at the error amplifier is given by

$$V_o' = V_{ref} - \beta V_o$$

Case (i): $V_o \uparrow$, $\beta V_o \uparrow$, $V_o' \downarrow$ to decrease V_o

Case (ii): $V_o \downarrow$, $\beta V_o \downarrow$, $V_o' \uparrow$ to increase V_o

} $\because$ Q_1 is a emitter follower.

For an ideal op-amp

$$V_{ref} = \beta V_o$$

$$V_o = \frac{V_{ref}}{\beta}, \quad \beta = \frac{R_3}{R_2 + R_3}$$

[R_2 is used to get the f/b o/p]

$$V_o = \frac{(R_2 + R_3)\, V_{ref}}{R_3}$$

$$\boxed{V_o = \left(1 + \frac{R_2}{R_3}\right) V_{ref}} \rightarrow (1)$$

Eq^n (1) Reveals that the o/p voltage is dependent on the stable values V_{ref} & standard R_2, R_3 values. Thus V_o is maintained stable.

Draw back of series op-amp regulators:-

(i) The pass transistor can be destroyed by excessive load current if the load is accidently shorted.
To avoid this current limiting circuit must be added to a series regulator.

(ii) No Thermal protection.

IC Voltage Regulators:-

when the discrete circuit is completely incorporated on a monolithic silicon chip, it is called an IC regulator.

Advantages of IC Regulators:-

(i) low cost
(ii) High Rediability
(iii) Reduction in size
(iv) Excellent performance
(v) Versatile
(vi) Provision for both voltage & current boosting.
(vii) Provides short circuit protection.
(viii) provides thermal shutdown feature.

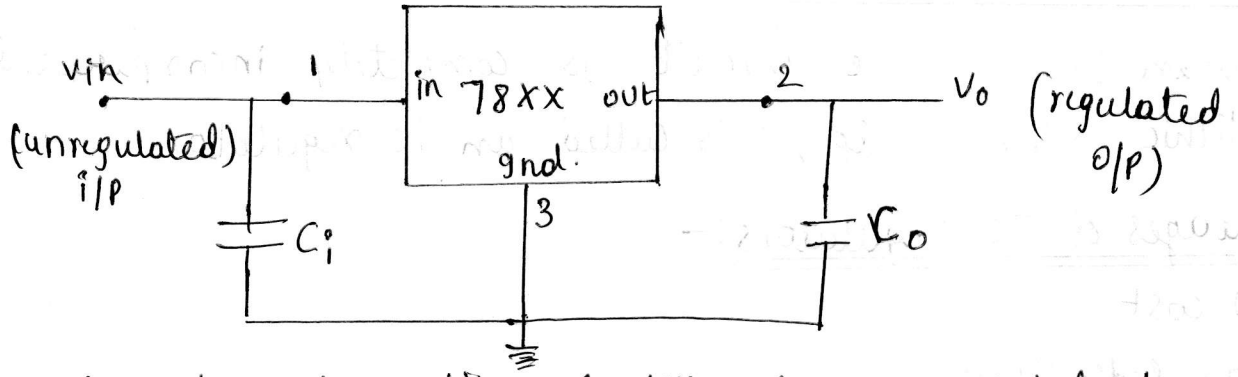
Fixed Voltage regulators (Series regulation) fixed)

78XX series regulators are 3 terminal positive fixed o/p voltage regulator. There are seven o/p voltage options available in this series as below along with maximum allowable i/p v/g.

Voltage options available in 78XX series

Device type	o/p voltage (V)	max. allowable i/p v/g Vin (V)
7805	5	35
7806	6	
7808	8	
7812	12	
7815	15	
7818	18	
7824	24	→ 40

The standard representation of the 3 terminal positive monolithic regulator is shown below.



The transformed rectified & filtered unregulated dc voltage is applied as the i/p V_i to the regulator. The o/p V_o is a regulated (constant) dc voltage. The difference $(V_{in} - V_o)$ is called the drop out voltage & is typically 2V.

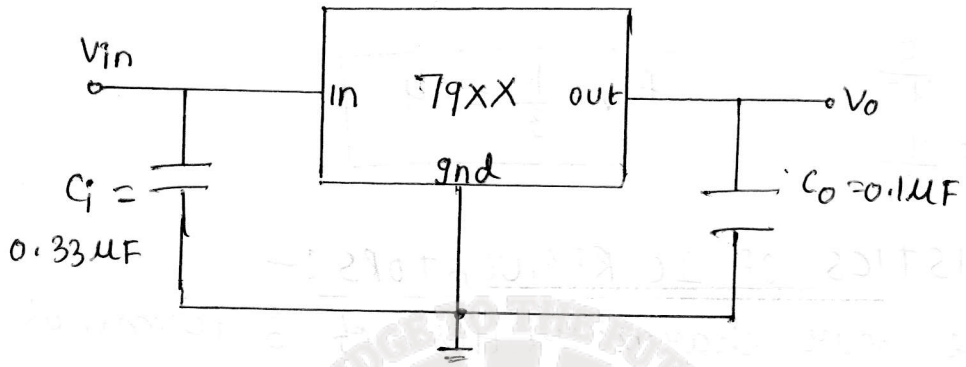
The capacitor [C_i] is recommended between ~~to~~ be connected between input pin 1 and ground to cancel the inductive effects when the regulator is located at an appreciable distance from the power supply. [$C_i = 0.33\mu f$]

The capacitor [C_o] is recommended between the o/p pin & ground to improve the transient response [$C_o = 0.1\mu f$]

79XX series regulators are 3 terminal negative fixed o/p regulators. This series has two additional o/p options as compared to 78XX series. The two additional options are -2V & -5.2V, as shown with max allowable i/p voltage.

Device type	o/p voltage (V)	max. allowable i/p V/g (V)
7902	-2	
7905	-5	
7905.2	-5.2	
7906	-6	
7908	-8	-35
7912	-12	
7915	-15	
7918	-18	
7924	-24	→ -40.

The standard representation of the 3 terminal -ve monolithic regulator is shown. It has all the salient features of 78XX series



78XX and 79XX are of motorola products named as MC 78XXC and MC 79XX C

MC → motorala
78 → +ve voltage
XX → Voltage
C → Commerical

The National Semiconductor also produces 3 terminal IC regulators in LM series

LM 100 series -55°C to +125°C
LM 200 series -25°C to +85°C
LM 300 series 0°C to +70°C

The popular series are LM340 +ve regulators and LM320 -ve regulator with rating comparable to 78XX & 79XX series.

PROBLEM:-

① In the series voltage regulator $R_2 = 2K\Omega$, $R_3 = 1K\Omega$, $V_Z = 6V$ & $V_{BE} = 0.7V$. what is the regulated o/p voltage

$$V_0 = \left[1 + \frac{R_2}{R_3}\right][V_Z + V_{BE}]$$

$$= \left[1 + \frac{2K}{1K}\right][6 + 0.7]$$

$$= 3[6.7]$$

$$\boxed{V_0 = 20.1V}$$

② In the series voltage regulator, $R_2 = 30K\Omega$, $R_3 = 10K\Omega$. what is the feedback gain

Sol^n:- $\beta = \frac{R_3}{R_2 + R_3} = \frac{10K}{10K + 30K}$

$= \frac{10}{40}$

$\beta = \frac{1}{4}$

$$\boxed{A_v = \frac{1}{\beta} = 4}$$

CHARACTERISTICS OF IC REGULATORS :-

There are four characteristics of 3 terminal IC regulator

① **V_o :** The regulated o/p voltage is fixed at a value as specified by the manufacturer.

② **$|V_{in}| \geq |V_o| + 2$:** The unregulated i/p voltage must be atleast 2V more than the regulated o/p voltage eg:- if $V_o = 15V$, $V_{in} = 17V$ i.e atleast 2V of drop out voltage.

③ **$I_o(max)$:** The load current may vary from 0 to rated maximum o/p current. The IC is usualy provided with heat sink, otherwise it may not provide the rated maximum o/p current.

④ **Thermal shutdown :-** The IC has a temperature sensor (built in) which turns off the ic when it becomes too hot (usually 125°C to 150°C). The o/p current will drop out and remain until the IC is cooled significantly

Line regulation $= \frac{\Delta V_o}{\Delta V_{in}}$, unit can be mV (or) %.

Typical value is 3mV

load regulation $= \frac{\Delta V_o}{\Delta I_L}$, unit can be mV (or) %.

Typical value is 15mV for $5mA < I_o < 1.5A$

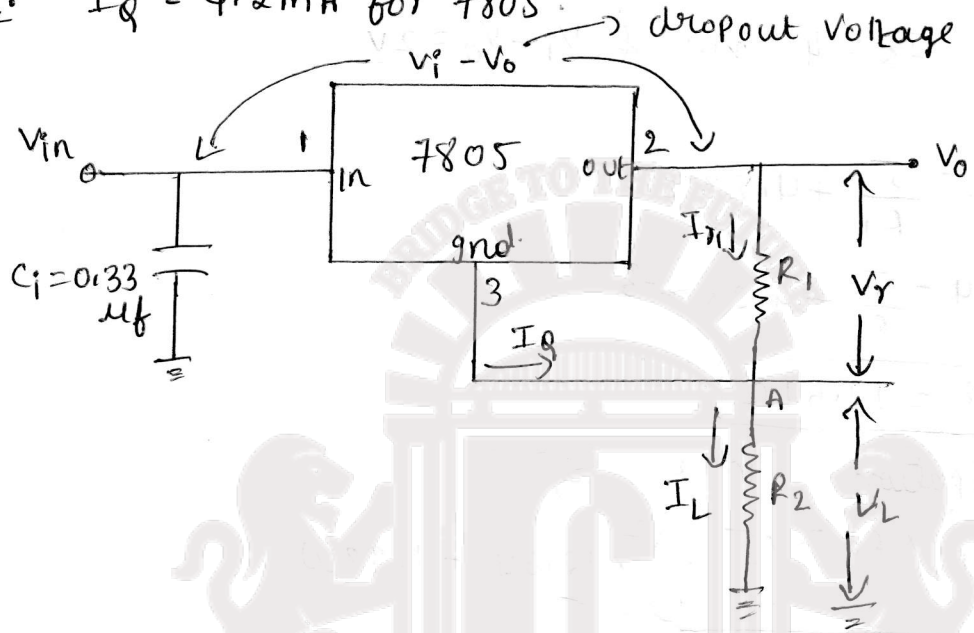
Ripple rejection $= \frac{\Delta V_{rs}}{\Delta V_{ro}}$, Typical value is 78db

For 7805 IC

Current Source :-

The 3 terminal fixed voltage regulator can be used as a current source. Figure shows the 7805 regulator used as a current source. The current I_Q represents the quiescent current that flows out of pin 3 which is typically 4.2mA for 7805.

NOTE :- $I_Q = 4.2mA$ for 7805.



V_R is the voltage at pin 2 w.r.t pin 3 which is 5V

$\therefore V_r = 5V = I_{R_1} * R_1$

$I_{R_1} = \frac{5V}{R_1}$ amps → (1) we have $I_Q = 4.2mA$ → (2)

Applying KCL at node A, we have

$I_L = I_{R_1} + I_Q$

Substituting the value of I_{r_1} & I_Q

$I_L = \frac{5A}{R_1} + 4.2mA$

$I_L = \frac{5}{R} + (4.2 \times 10^{-3})$ → (3)

let us consider a case where the load current $I_L = 1A$ is to be delivered to a load resistance of $R_L = 5\Omega$.

From eqn (3)

$1A = \frac{5}{R_1} + 4.2 \times 10^{-3}$

$\boxed{R_1 = 5\Omega}$

Power dissipation in R_1 is $P_R = I_{R_1}^2 \times R_1 = 1^2 \times 5 = 5W$

$\boxed{R_L = 5\Omega}$

The $V_0 = V_r + V_L = 5 + I_L R_L = 5 + 5 = 10V$

PROBLEM:-

① Design a current source using 7805 Voltage regulator to deliver a load current of 0.4A into a 56Ω/10W load

Sol^n:- $I_L = 0.4A$, $R_L = 56\Omega$

For 7805, $I_Q = 4.3mA$ & $V_i - V_0 = 2V$

we have

$$I_L = \frac{5}{R_1} + 4.2 \times 10^{-3}$$

$$0.4 = \frac{5}{R_1} + 4.2 \times 10^{-3}$$

$$\boxed{R_1 = 12.64\Omega}$$

Power dissipation in R_1 is,

$$P_{R_1} = I_{R_1}^2 \times R_1 = \left(\frac{5}{12.64}\right)^2 \times 12.64 = 1.98W$$

$$\boxed{P_{R_1} = 1.98W}$$

Power dissipation in load is

$$P_L = I_L^2 R_L = (0.4)^2 \times 56\Omega = 8.96W$$

$$\boxed{P_L = 8.96W}$$ ∴ 10W load resistor given is suitable.

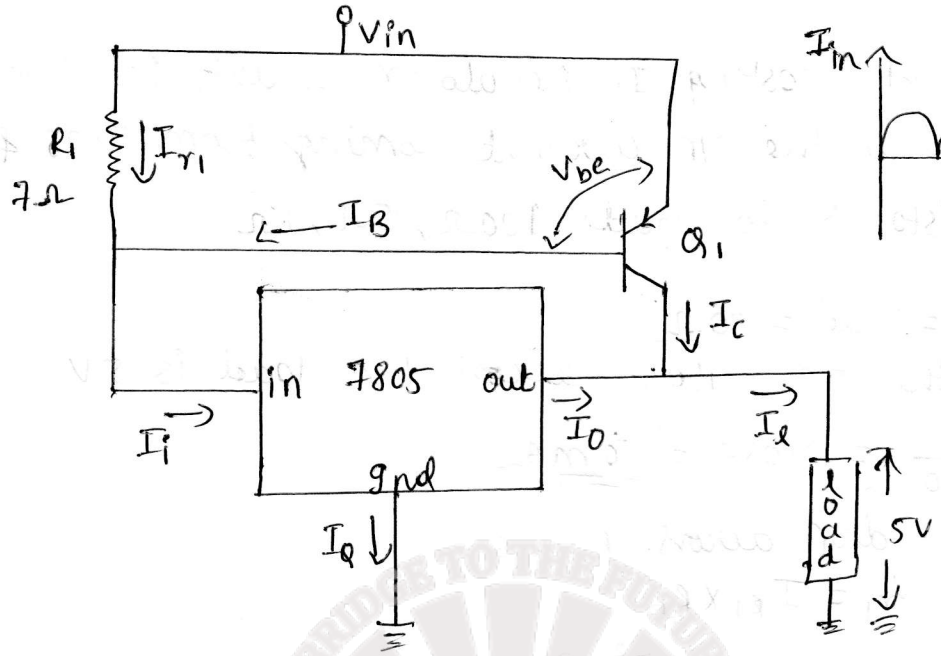
$$V_0 = V_r + V_L = I_{R_1} \times R_1 + I_L \times R_L$$

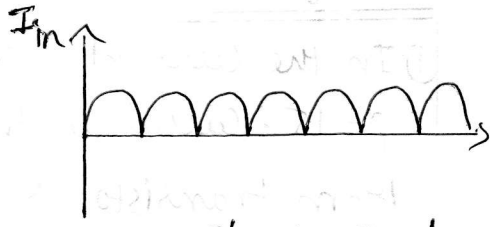
$$= 5 + (0.4)(56)$$

$$\boxed{V_0 = 27.4V}$$

Boosting IC Regulator output current:-

It is possible to boost the O/P current of a 3 terminal regulator by simply connecting an external pass transistor in parallel with the 3-terminal regulator as shown.





O/P current of the unregulated supply

when I_{in} is low, the drop across the resistor R_1 is less and is insufficient (<0.7V) to turn on transistor Q_1 and regulator itself is able to supply the load current.

However as the I_{in} increases, the voltage drop across R_1 increases when this voltage drop is approximately 0.7V, the transistor Q_1 turns on, & supplies the extra current. since $V_{BE(on)} = 0.7V$ remains constant, the excess current from Q_1 comes in its amplified form.

$$I_L = I_O + I_C \rightarrow (1), \quad I_C = \beta I_B \rightarrow (2)$$

For a regulator $I_O = I_i - I_Q$

$$I_O \cong I_i \quad (\because I_Q \text{ is very small}) \rightarrow (3)$$

Also $I_{R_1} + I_B = I_i$

$$I_B = I_i - I_{R_1}$$

$$I_B = I_i - \frac{V_{BE(on)}}{R_1} \rightarrow (4)$$

we have from (1)

$$I_L = I_O + I_C$$

$$I_L = I_O + \beta I_B$$

$$= I_O + \beta\left(I_i - \frac{V_{BE(on)}}{R_1}\right) \qquad I_i = I_O$$

$$I_L = I_O + \beta I_O - \frac{\beta V_{be(on)}}{R_1}$$

$$\boxed{I_L = (\beta+1) I_O - \frac{\beta V_{BE(on)}}{R_1}}$$

PROBLEMS:-

(1) In the current Boosting IC regulator circuit, let $V_{be(on)} = 1V$, $\beta = 15$. Calculate the o/p current coming from 7805 & I_C coming from transistor Q_1 for loads 100Ω, 5Ω, 1Ω

Sol^n:- Case (i) = Load = 100Ω

For 7805, the o/p voltage across the load is 5V

$$I_L = \frac{5V}{100} = 0.05A = 50mA$$

The voltage drop across R_1 is

$$V_{R_1} = I_{R_1} \times R_1$$

$$= 50 \times 10^{-3} \times 7\Omega$$

$$V_{R_1} = 350mV$$

which is less than 0.7V, Hence Q_1 is off.

So, $I_L = I_O = I_i = 50mA$

& $\boxed{I_C = 0}$

Case (ii):- $R_L = 5\Omega$

$$I_L = \frac{5}{5} = 1A$$

$I_L = I_{R_1}$, $V_{R_1} = I_{R_1} \times R_1$

$V_{R_1} = 7V$, Thus the Q_1 is on.

$$I_L = (\beta+1) I_O - \beta \frac{V_{be(on)}}{R_1}$$

$$I_L + \beta \frac{V_{be(on)}}{R_1} = 16 I_O$$

$$16 I_O = 1 + \frac{15 \times 0.7}{5}$$

$$I_O = 156.25mA$$

$$I_C = I_L - I_O$$

$$= 1A - 156.25mA$$

$$I_C = 843.75mA$$

$$I_i = I_{R_1} + I_B$$

$$= 1A + \frac{843.75mA}{15}$$

$$I_i = 1.05625A$$

Case (3) :- $R_L = 1\Omega$

$$I_L = \frac{V_L}{R_L} = \frac{5V}{1\Omega} = 5A$$

Assume, $I_L = I_{r_1}$, $V_{r_1} = I_{R_1} \times R_1$

$= 5A \times 7\Omega$

$V_{r_1} = 35V$

$V_{r_1} \geq V_{BE(on)} \Rightarrow Q_1$ is on.

$I_L = I_0 + I_C$

$$I_L = (1+\beta) I_0 - \frac{\beta V_{be(on)}}{R_1}$$

$$5 + \frac{15 \times 0.7}{7} = 16 I_0.$$

$$\boxed{I_0 = 406.25mA}$$

$I_C = I_L - I_0$

$= 5 - 406.25mA$

$$\boxed{I_C = 4.5937A}$$

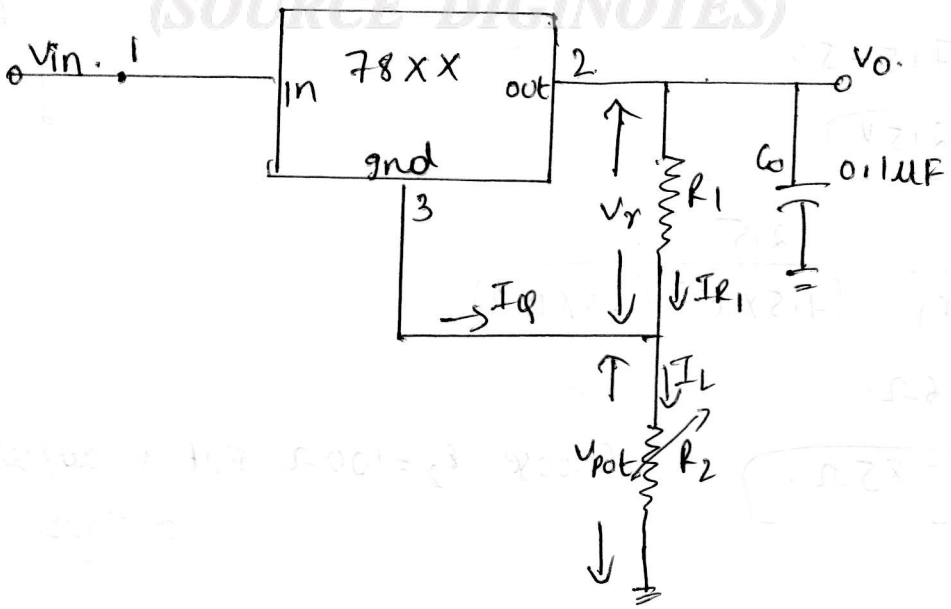
$I_i = I_{R_1} + I_B$

$= 5A + 0.130625$

$$\boxed{I_i = 5.130625A}$$

Fixed Regulator as adjustable Regulator :-

In certain applications we may need a variable regulat output voltage or an o/p voltage that is not available from the standard fixed voltage regulators. In such situations we can achieve adjustable o/p voltage using fixed voltage regulators, as shown.



The o/p voltage is

$$V_o = V_R + V_{pot}$$

$$= V_R + I_L R_2$$

$$V_o = V_R + (I_{R_1} + I_Q) R_2$$

$$V_o = V_R + I_{R_1} R_2 + I_Q R_2$$

$$V_o = V_R + \frac{V_R}{R_1} R_2 + I_Q R_2$$

$$V_o = \left[1 + \frac{R_2}{R_1}\right] V_R + I_Q R_2 \longrightarrow (1)$$

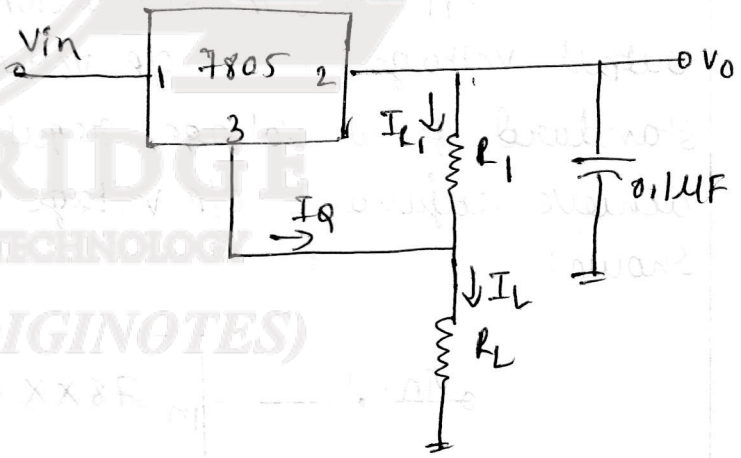
V_r is the regulated voltage b/w out & gnd pin.

The second term of eqn (1) can be made small by choosing R_2 small. The minimum value of $V_o = V_r$ when $R_2 = 0$.

∴ As $R_2 \uparrow$ the V_o also increases. Thus acheiving adjustable voltage

PROBLEM:-

(1) Find the value of R_2 to obtain $V_o = 7.5V$ using 7805 in fig. Choose $I_{R_1} = 25mA$.



For 7805, $I_Q = 4.2mA$

$$R_1 = \frac{V_R}{I_{R_1}} = \frac{5}{25 \times 10^{-3}} = 200\Omega$$

$$V_o = V_{POT} + V_r$$

$$V_{POT} = 7.5 - 5V$$

$$\boxed{V_{POT} = 2.5V}$$

$$R_2 = \frac{V_{pot}}{I_Q + I_{R_1}} = \frac{2.5}{(4.5 \times 10^{-3})(25 \times 10^{-3})}$$

$$R_2 = 85.6\Omega$$

Choose $\boxed{R_2 = 85\Omega}$

Choose $R_2 = 100\Omega$ pot & adjust it to $\cong 85\Omega$

723 General purpose Regulator :-

3 Pin regulator have the following limitations :-

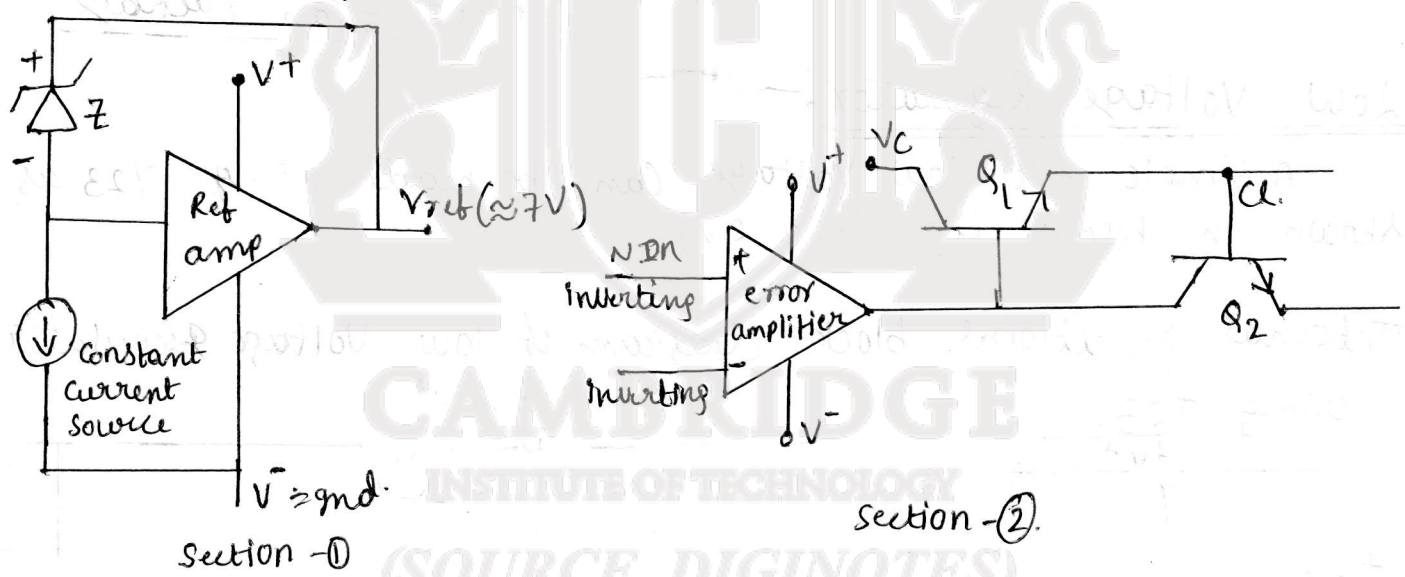
(1) NO short circuit protection.

(2) O/p voltage (+ve or -ve) is fixed. Range is limited in case of adjustable circuit

The O/p voltage of 723 regulator can be adjusted over a wide range of both +ve & -ve regulated voltage. This IC has low current driving capability but can be boosted to provide 5A (or) more by connecting external component. Another limitation of 723 regulator is that no thermal protection & also no short circuit current limits.

Functional block diagram of 723 General purpose Regulator

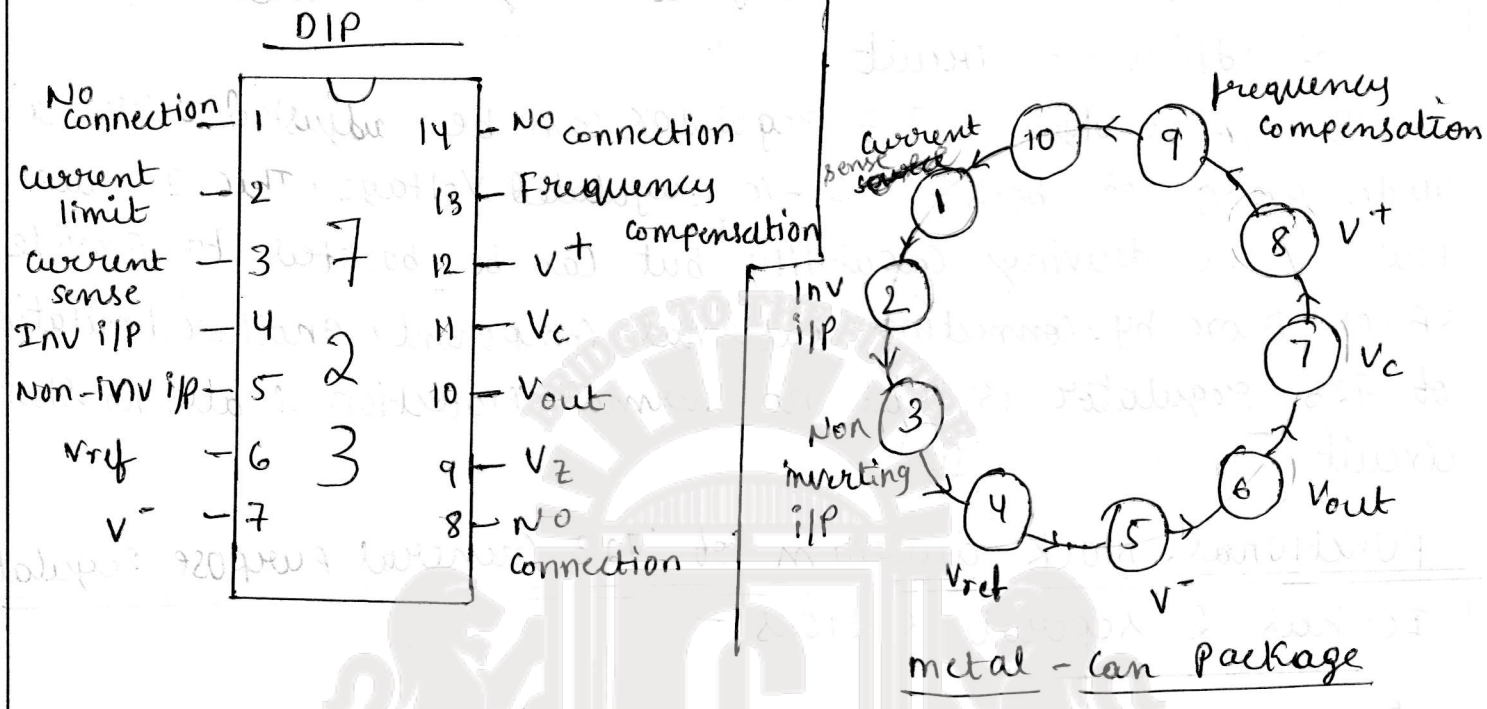
IC has 2 seperate sections :-



1) The zener diode, a constant current source & reference amplifier producing a fixed voltage of about 7V at the terminal V_{ref}. The constant current source fixes the zener to operate at a fixed point so that the zener O/p's a fixed voltage of about 7V, at the terminal V_{ref}.

2) The other section of the IC contains an error amplifier a series pass transistor Q_1 & a current limit transistor Q_2. The error amplifier compares a sample of the O/p voltage applied at the inverting i/p terminal to the reference voltage. V_{ref} is applied at the non-inverting i/p terminal.

The error signal controls the conduction of Q_1. The internal connections are not completely shown. 723 regulator IC is available in a 14 pin dual in-line package or 10 pin metal can as shown in fig

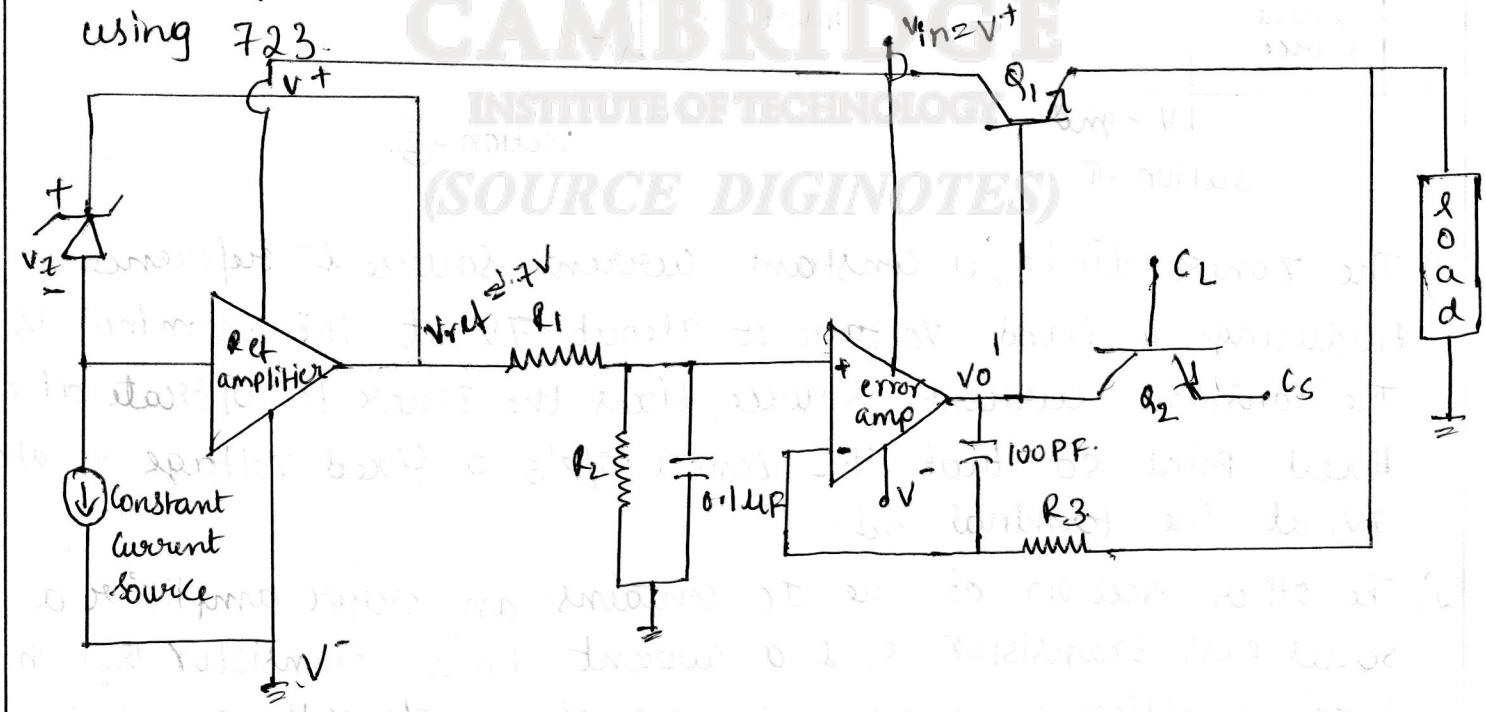


metal - can package

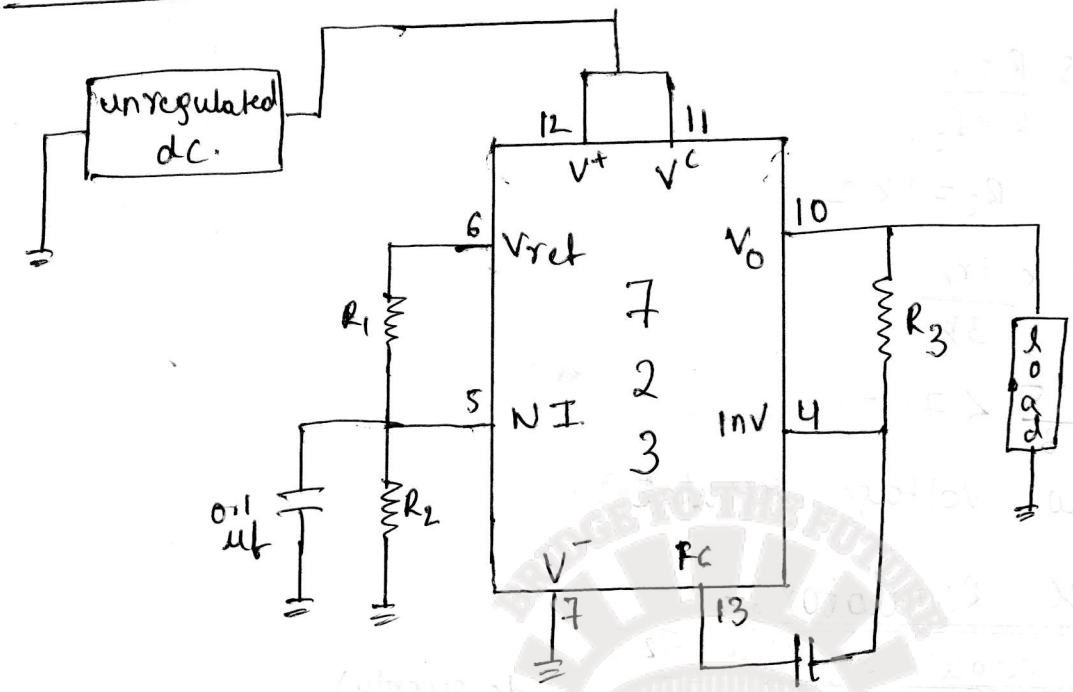
Low Voltage Regulator:-

A simple +ve low voltage can be made using 723 as shown in below fig (i.e 2V)

Internal functional block diagram of low voltage regulator using 723.



Functional Pin - Diagram:-



The output of the section 1 i.e V_{ref} is voltage divided by R_1 & R_2 & fed to non-inverting terminal.

∴ voltage at non-inverting terminal will be

$$V_{NI} = \frac{V_{ref} \cdot R_2}{R_1 + R_2}$$

The o/p of the error amplifier (i.e the difference b/w the ref i/p & the feed back signal) is used to control the pass transistor Q_1, so as to maintain the difference b/w the two i/p terminals of the error amplifier.

The transistor is an emitter follower so, it follows the i/p

$$V_o = \left(\frac{R_2}{R_1 + R_2}\right) \cdot V_{ref}.$$

If the o/p voltage becomes low, the voltage at the inverting terminal of error amplifier also goes down. Thus making o/p of error amplifier to become more +ve & drives Q_1 into more conduction. Thus current I_L is increased thus increasing the o/p voltage. Similarly if any increase in load voltage will get reduced.

The reference voltage is typically 7.15 voltage & the O/P voltage is

$$V_0 = 7.15 \frac{R_2}{R_1+R_2}$$

say $R_1 = 2k\Omega$ $R_2 = 1k\Omega$

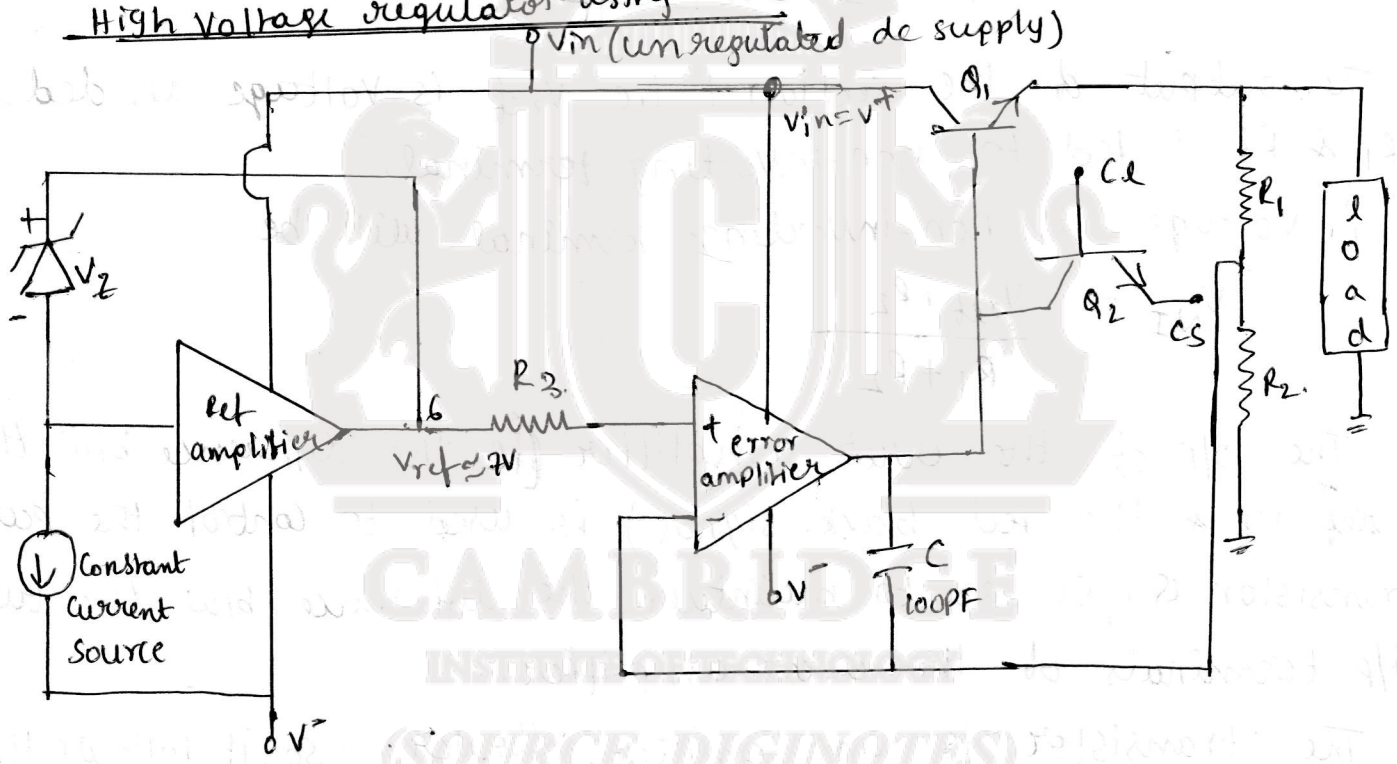
$$V_0 = 7.15 \times \frac{1k}{3k}$$

$$V_0 = \frac{7.15}{3} < 7.15$$

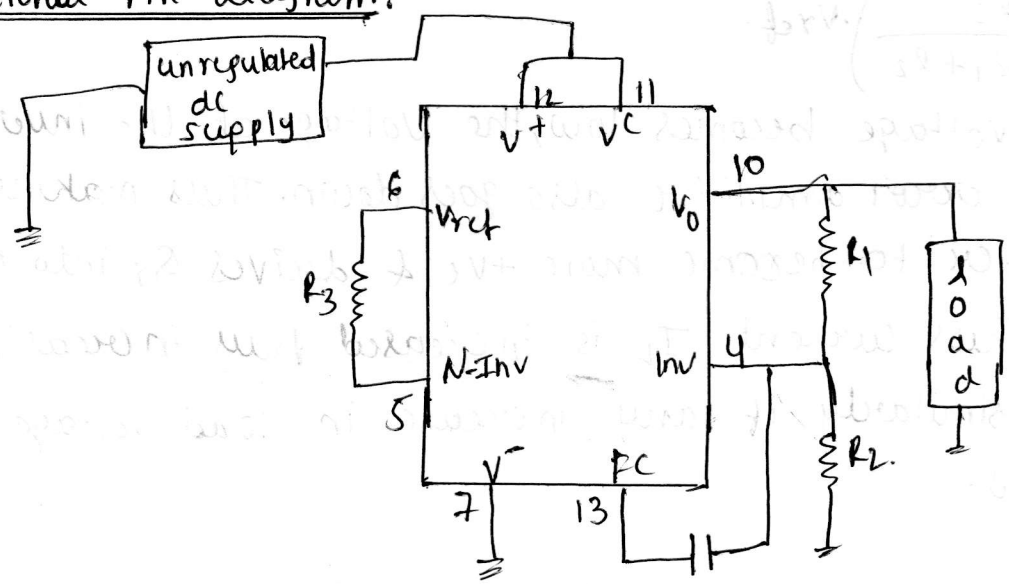
Thus low voltage regulator.

High Voltage Regulator:-

High voltage regulator using 723



Functional pin diagram:-



If we consider the internal circuit of high voltage regulator using 723, the reference voltage V_{ref} is directly connected to the non-inverting terminal through resistor R_3. The reference voltage appears across the non-inverting terminal & thus it acts as an non-inverting amplifier

The gain of the non-inverting amplifier $= \frac{1}{\beta}$

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$\therefore A_V = \frac{R_1 + R_2}{R_2}$$

$$\boxed{A_V = 1 + \frac{R_1}{R_2}}$$

we have,

$$A_V = \frac{V_o}{V_i}$$

$$V_o = A_V V_i$$

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_i$$

Here $V_i = V_{ref}$.

$$\therefore \boxed{V_o = \left(1 + \frac{R_1}{R_2}\right) V_{ref}} \rightarrow (2)$$

Case (i) if $R_1 = R_2 = 0$.

$$\boxed{V_o = V_{ref} = 7V}$$

Case (ii)

if $R_1 = 1K$, $R_2 = 2K$.

$$V_o = 7\left[1 + \frac{1}{2}\right]$$

$$V_o = 7[1.5]$$

$$\boxed{V_o = 10.5V}$$

Case (iii) if $R_1 = 2K$, $R_2 = 1K$.

$$V_o = 7[1 + 2]k.$$

$$\boxed{V_o = 21V}$$

Thus we can conclude it acts as a high voltage regulator.

~~End of Module 4 [PART - B]~~

Switching regulator or (switch mode power supply)

Not Included in Syllabus

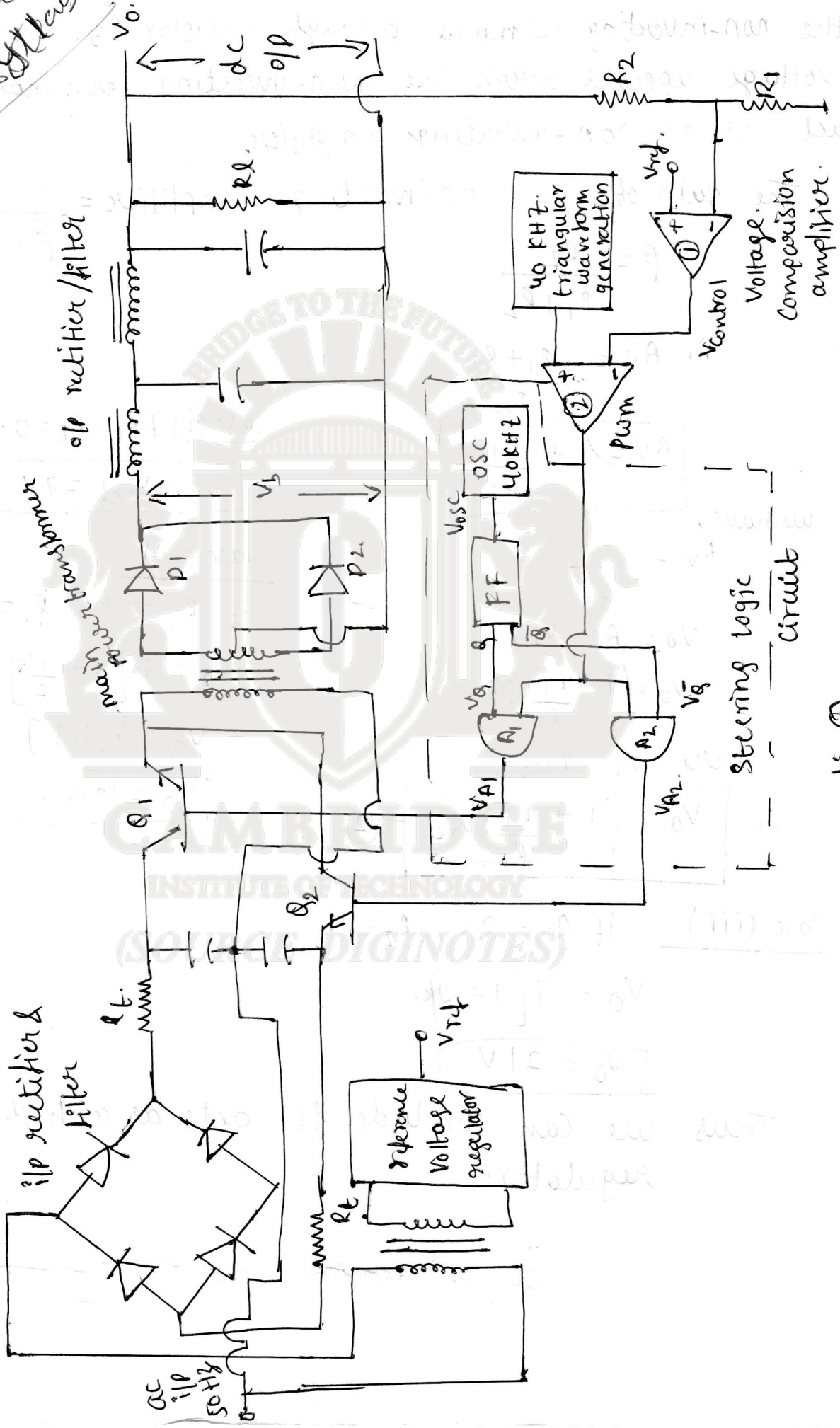
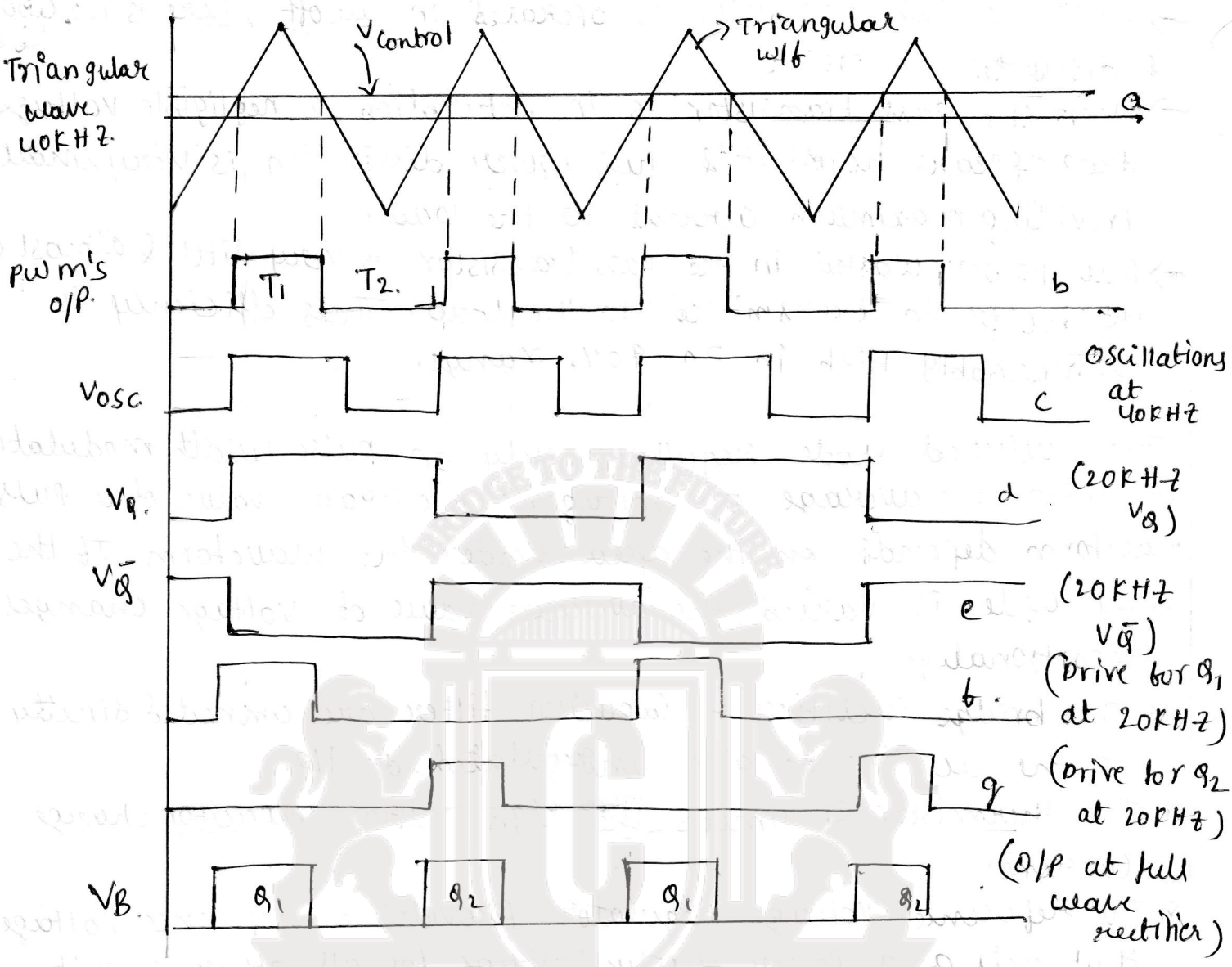


fig ①

fig (b)



The limitation of linear voltage regulator (series) are :-

(1) step down transformer is bulky & expensive.

(2) Since low line frequency (50HZ), large values of capacitor needs to be used to attenuate ripple.

(3) The i/p voltage must be greater than o/p voltage, greater the difference, greater is the power dissipation in the pass transistor.

(4) Efficiency of linear voltage regulator is low.

Switched regulators overcome these difficulties.

→ In case of series regulator the pass transistor is operated in linear region to provide a controlled voltage drop across it with a steady dc current flow.

→ In case of switched-mode regulator, the pass transistor is used as a "controlled switch" & is operated at either cut-off (or) saturation state. Thus greater efficiency is acheived.

→ when the pass transistor is operated in cutoff, there is no current & dissipates no power.

→ when the pass transistor is in saturation, a negligible voltage drop appears across it & thus power dissipation is very small providing maximum current to the load.

→ Thus power wasted in the pass transistor is very little & almost all the power in transmitted to the load. Thus efficiency is remarkably high in 70-90% range.

The switched mode regulators rely on pulse width modulation to control the average o/p voltage. The average value of a pulse waveform depends on the area under the waveform. If the duty cycle is varied, the average value of voltage changes proportionally

* The bridge rectifier & capacitor filter are connected directly to the ac line to give unregulated dc i/p.
* The thermistor R_t limits the high initial capacitor charge current.
* The reference voltage regulator provides a reference voltage that acts as a power supply voltage for all other circuit.

The current drawn from V_{ref} is very small & thus power loss in series pass regulator i.e reference voltage regulator is less & thus improving the efficiency of the switched mode power supply (SMPS).

* Q_1 & Q_2 are alternatively switched on and off at 20KHz. These transistors are either fully on ($V_{ce\,sat} \sim 0.2V$) or cut off, so they use very little power.
* These transistor drive the main transformer. The secondary is center tapped & full wave rectification is acheived by diodes D_1 & D_2. This unidirectional square wave is next filtered through a two stage LC filter to produce o/p voltage V_o.

The regulation (maintaining stability in the o/p voltage) is acheived by the feedback circuit consisting of a pulse width modulator & steering logic circuit. The o/p is sampled by a R_1 R_2 divider & a fraction is compared with fixed reference voltage V_{ref} in comparator 1. The o/p of this voltage comparator is called $V_{control}$.

$V_{control}$ is applied to the (-) i/p terminal of comparator 2 & a triangular waveform of frequency 40KHz is applied to the (+) i/p terminal. Here high frequency triangular wave is used to cancel ripple.

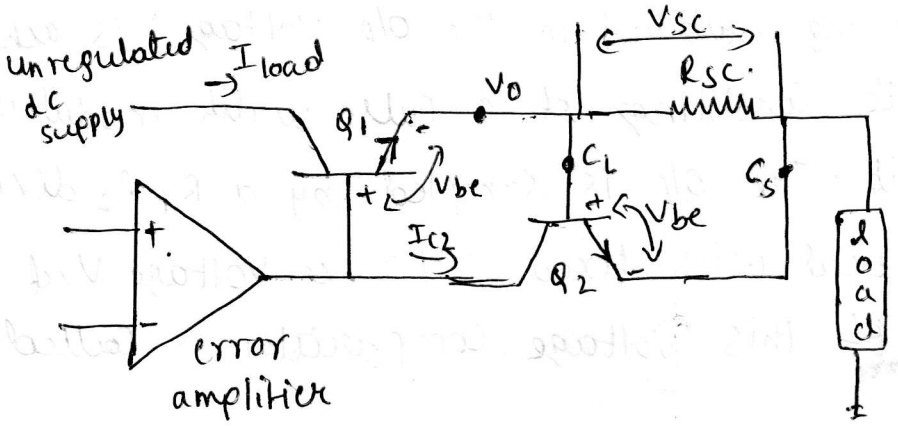
The o/p of comparator 2 is V_A (square wave) whose duty cycle varies with $V_{control}$ which in turn varies with the variation in V_A. The V_A drives the steering logic circuit.

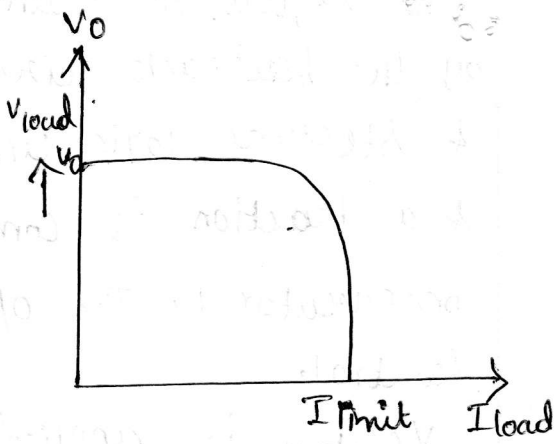
The o/p's of the and gate V_{A_1} & V_{A_2} are used to drive Q_1 & Q_2. Depending upon whether Q_1 (or) Q_2 is on the w/f at the i/p of the transformer will be a square wave as shown in fig ①. The rectified o/p is shown in fig ⓑ.

Current limit protection:-

The application circuit of 723 voltage regulator i.e low & high voltage regulators does not have current limit protection. If the load demands more current eg under short circuit conditions, the IC provides it at a constant voltage (o/p) getting hotter. This will burn IC.

The IC thus needs to be provided with a current limit facility. Current limit means to prevent the load current increasing above the preset value. This can be best understood with the help of a circuit diagram & the characteristic curve of a current limited power supply is shown





If we check the characteristic curve the O/P voltage V_O is maintained constant for load current below I_{limit}. As current approaches to the I_{limit}, the O/P voltage drops. The voltage is made to drop by connecting a resistor R_{SC} as shown b/w the terminals C_L & C_S, when the I_L is increasing the drop across the transistor, V_{be} is also increasing. The value of R_{SC} is so choosen that $R_{SC} = \frac{V_{be}}{I_{limit}}$, V_{be} here is 0.5V, we can get the I_{limit} from the data sheet & determine R_{SC}.

When the drop across the resistor R_{SC} approaches $V_{be}=0.5V$ the transistor Q_2 will start conduction providing a path for the load current to flow that limiting the flow of current through Q_1, As the current in Base of Q_1 decreases. Thus nullifying the increase in load current.

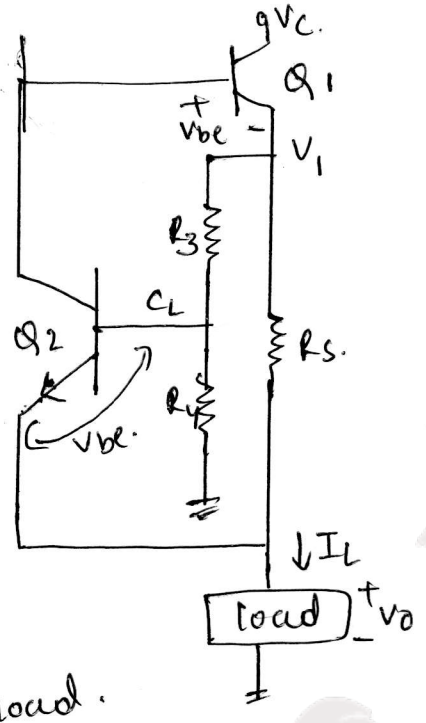
This method of current limiting is also reffered to as current sensing technique.

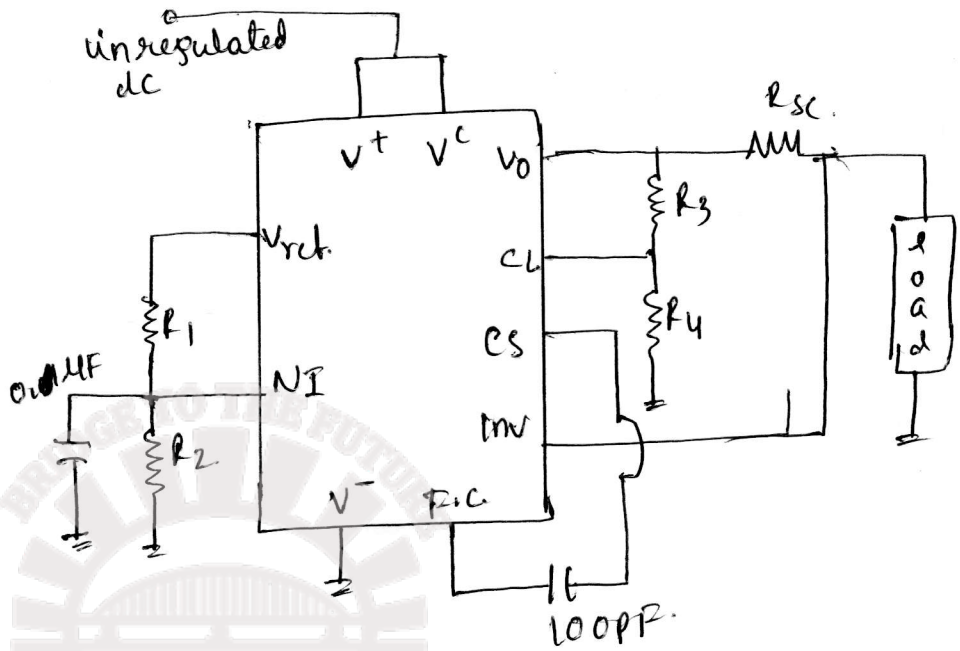
Current fold :-

In current sensing technique the load current is maintained at a preset value & over load occur the O/P voltage drops to zero. This is equivalent to short occur at the load. If there is a short at the load, the maximum current does flow through the regulator, destroying the IC. To prevent this, a method which limit the short circuit current & yet allow higher current to load must be devised

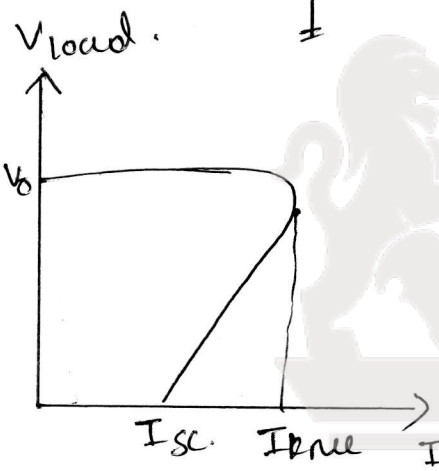
The method is known as "current foldback"

Consider the current foldback characteristic curve.





Current fold back circuit



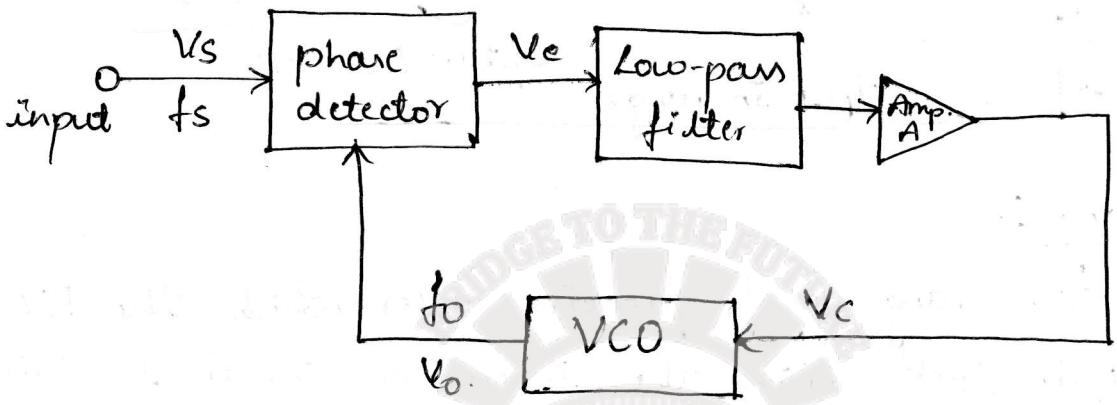
As current demand increase, the voltage is maintained constant till the current approches the preset value (I_{knee}). If the current demand leads this value, both o/p voltage & o/p current decreases

Consider the circuit, the voltage at C_L is divided by R_3 & R_4 n/w, the transistor Q_2 will conduct only when the drop across the resistor R_{sc} is large enough to provide a voltage of 0.5 V across C_L & C_S terminal. Once the transistor Q_2 starts conducting the conducting of Q_1 reduces & the voltage V_1 will reduce. This V_1 will make changes in the drop at C_L (decreases) Thus drop at C_L will be smaller compared to drop at C_S which increases V_{be} of Q_2 & conduction of Q_2 is increased.

NOTE: Refer class notes for Dual power supply using voltage regulators.

← End of module-4B →

→ Phase - Locked Loops :- [PLL]

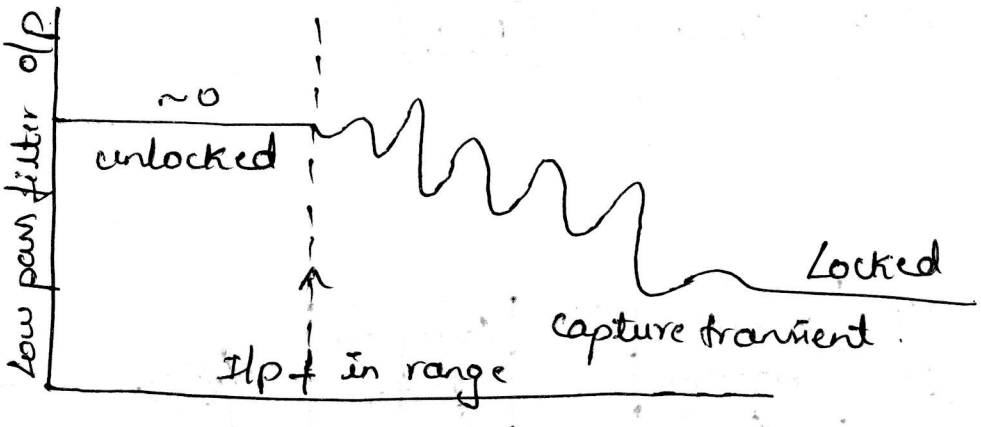


Block schematic of the PLL

The feedback system consists of
1) phase detector / comparator
2) A low pass filter
3) An error Amplifier
4) A Voltage controlled oscillator (VCO)

- The input signal V_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V_o of the VCO.
- The high frequency component is removed by low pass filter.
- If the two signals differ in frequency (or) in phase, an error voltage V_e is generated.
- V_c signal shifts the VCO frequency to reduce frequency b/w f_s and f_o.
- The VCO continues to change frequency till its o/p frequency is equal to i/p signal frequency. Then the ckt is said to be locked.

The important definitions related to PLL are:



1) <u>Lock-in Range</u> :-

The range of frequencies over which the PLL can maintain Lock with the incoming signal is called lock-in Range.

2) <u>Capture Range</u> :-

The Range of frequencies over which the PLL can acquire lock with an i/p signal is called Capture Range.

3) <u>pull-in time</u> :-

The total time taken by the PLL to establish lock is called pull-in time.

~~PHASE Detector~~

Phase Detector / Comparator

There are two types of phase detector used analog and digital.

Analog Phase Detector:

→ The principle of analog phase detection using Switch type detector as shown in fig(a) below.

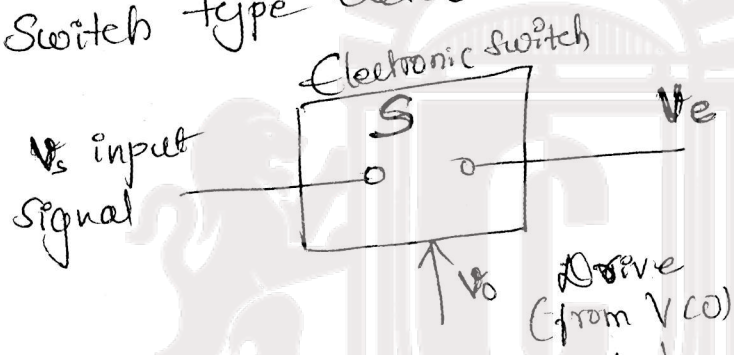


fig (a)

→ An electronic switch 'S' is opened and closed by signal coming from VCO [square wave] as show in fig (b)

→ The input signal is, therefore chopped at a repeatation rate determined by VCO frequency.

→ fig (c) shows the input signal V_s assumed to be in phase ($\phi = 0°$) with VCO o/p V_c.

→ Since 'S' is closed only when VCO o/p is positive the o/p waveform V_e will be half sinusoids.

→ similarly, the o/p waveform for $\phi = 90°$ and $\phi = 18$ as shown in fig (d) & (e)

→ This phase detector called a half wave detector

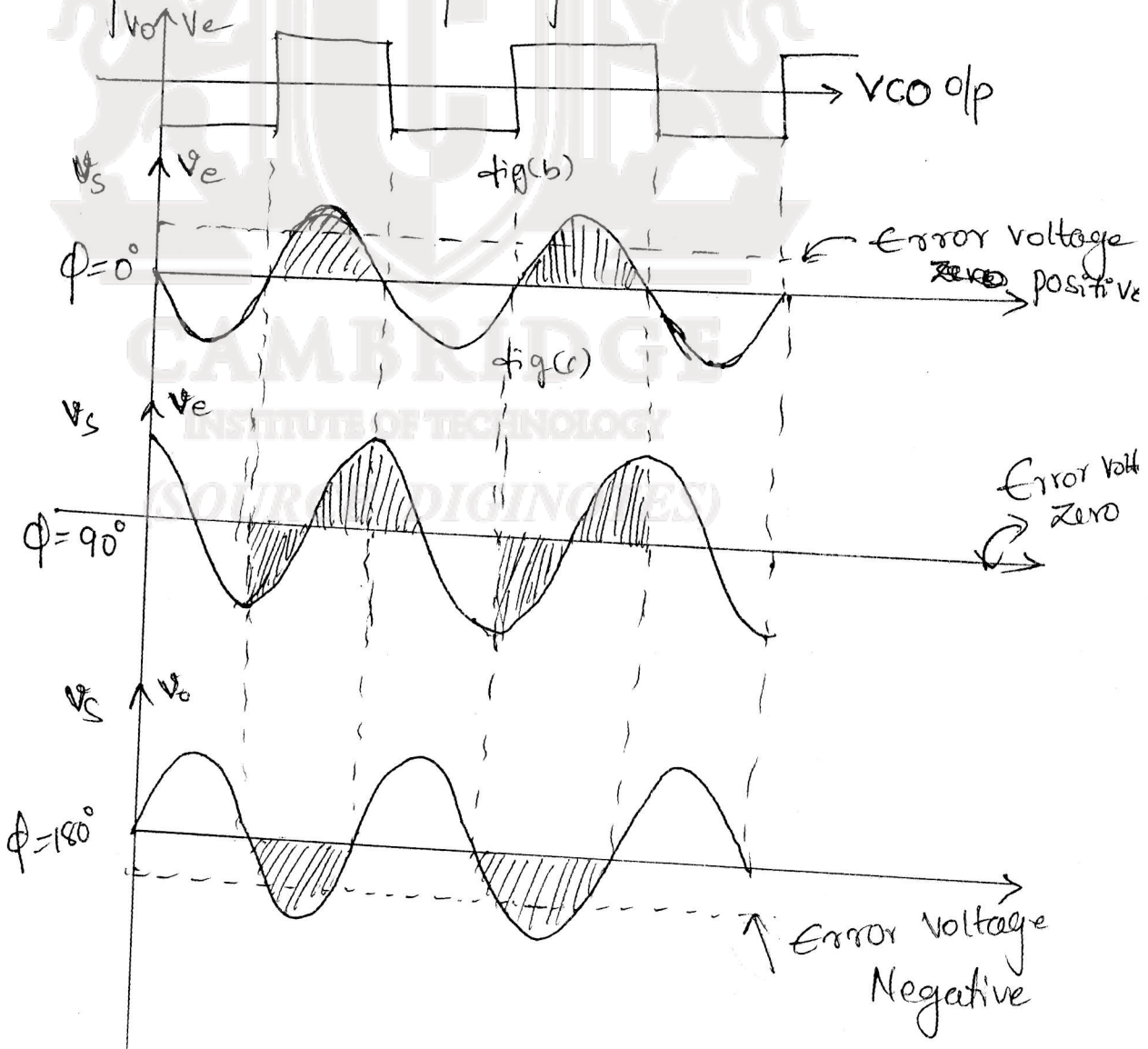
→ Since the phase information for only one-half of ~~phase detector~~ the waveform detected and averaged

→ The o/p of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line.

→ ~~Remarks~~

→ The error voltage is zero when the phase shift b/w ~~two~~ the two inputs is 90°.

→ perfect lock, the VCO o/p should be 90° out of phase with respect to the input signal.



Digital Phase ~~Dector~~ Detector

→ Digital type XOR phase detector [It uses CMOS type 4070 Quad. 2-input gate]

→ The o/p of the XOR gate is high when only one of the inputs signals ~~are square waves~~. f_s (or) f_o is high.

→ This type of detector is used when both the input signals are square waves.

→ ~~The~~ The i/p & o/p waveforms for $f_s = f_o$ are shown in fig (b)

→ from this f_s is leading f_o by ϕ degrees.

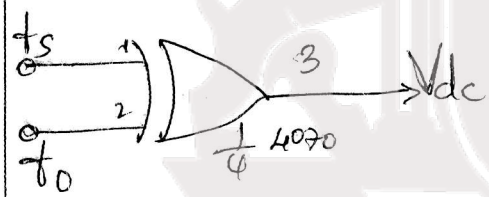


fig (a)
EXOR phase detector

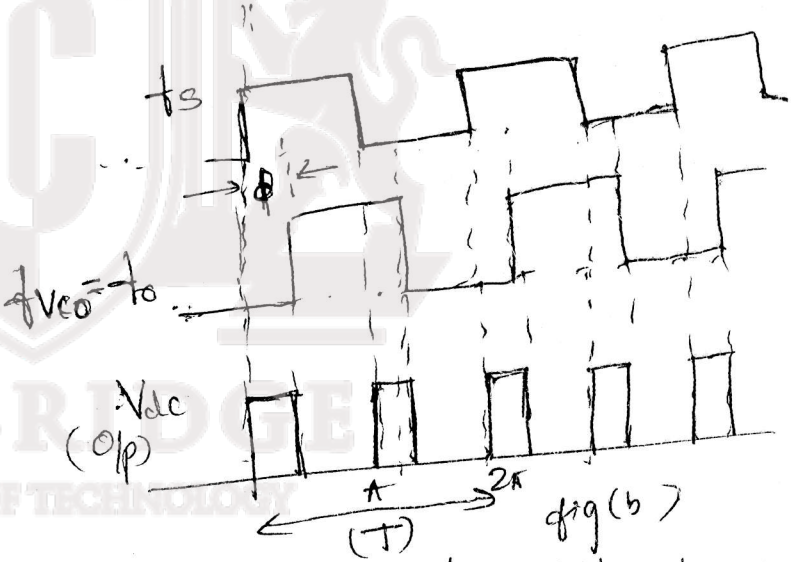
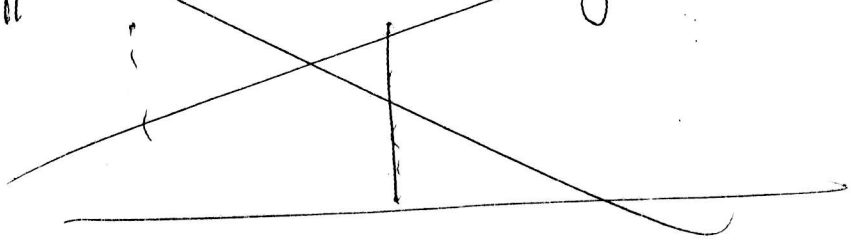
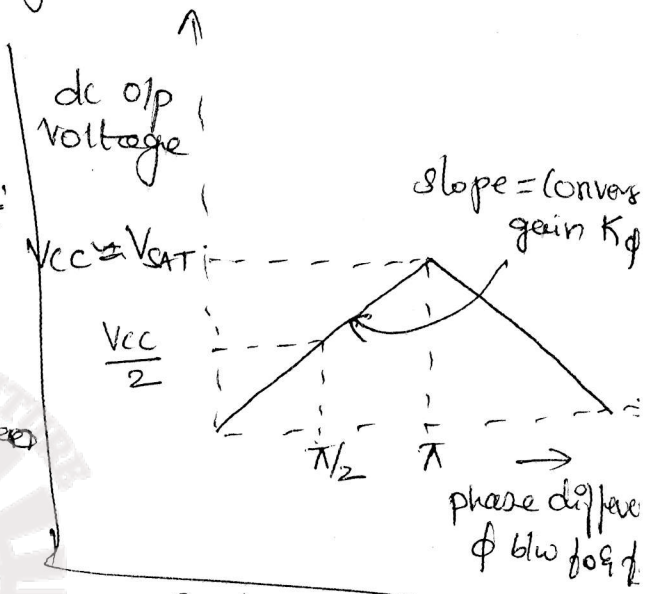


fig (b)
i/p & o/p waveforms

→ ~~The variation of dc o/p voltage with phase difference ϕ is shown in fig (c)~~



→ The variation of dc o/p voltage with phase difference 'ϕ' is shown in fig. below.



→ It can be seen that the maximum DC o/p voltage occurs when the phase difference is 'π'

→ because the o/p of the gate remains high throughout.

→ The slope of the curve gives the conversion ratio K_ϕ of the phase detector.

So, the conversion Ratio K_ϕ for a supply voltage $V_{CC}=5V$ is

$$\boxed{K_\phi = \frac{5V}{\pi} = 1.59\ V/rad} \simeq \boxed{K_\phi = \frac{V_{CC}}{\pi}}$$

Edge-triggered phase detector:

$\boxed{DC < 50\%}$

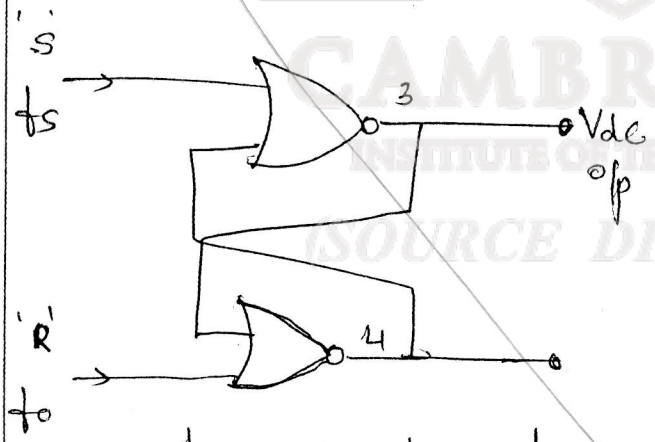


fig (a) Edge triggered phase detector

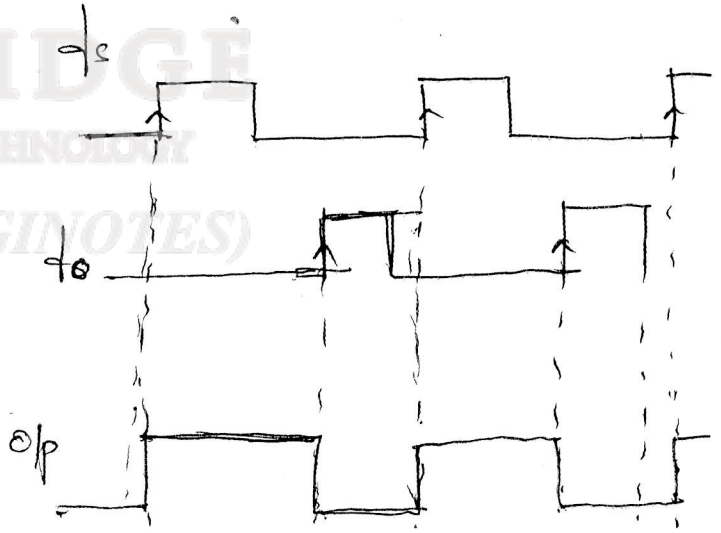


fig (b) i/p & o/p wave form.

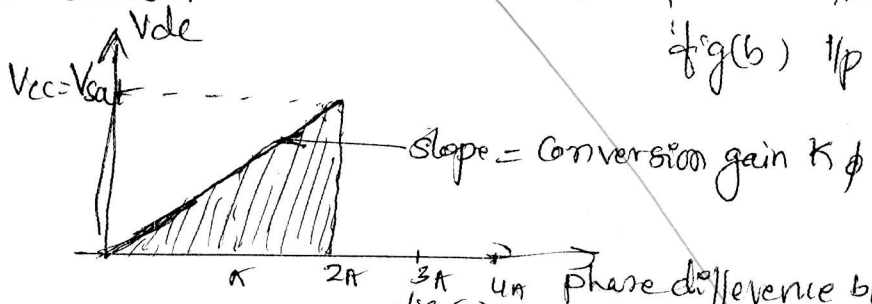
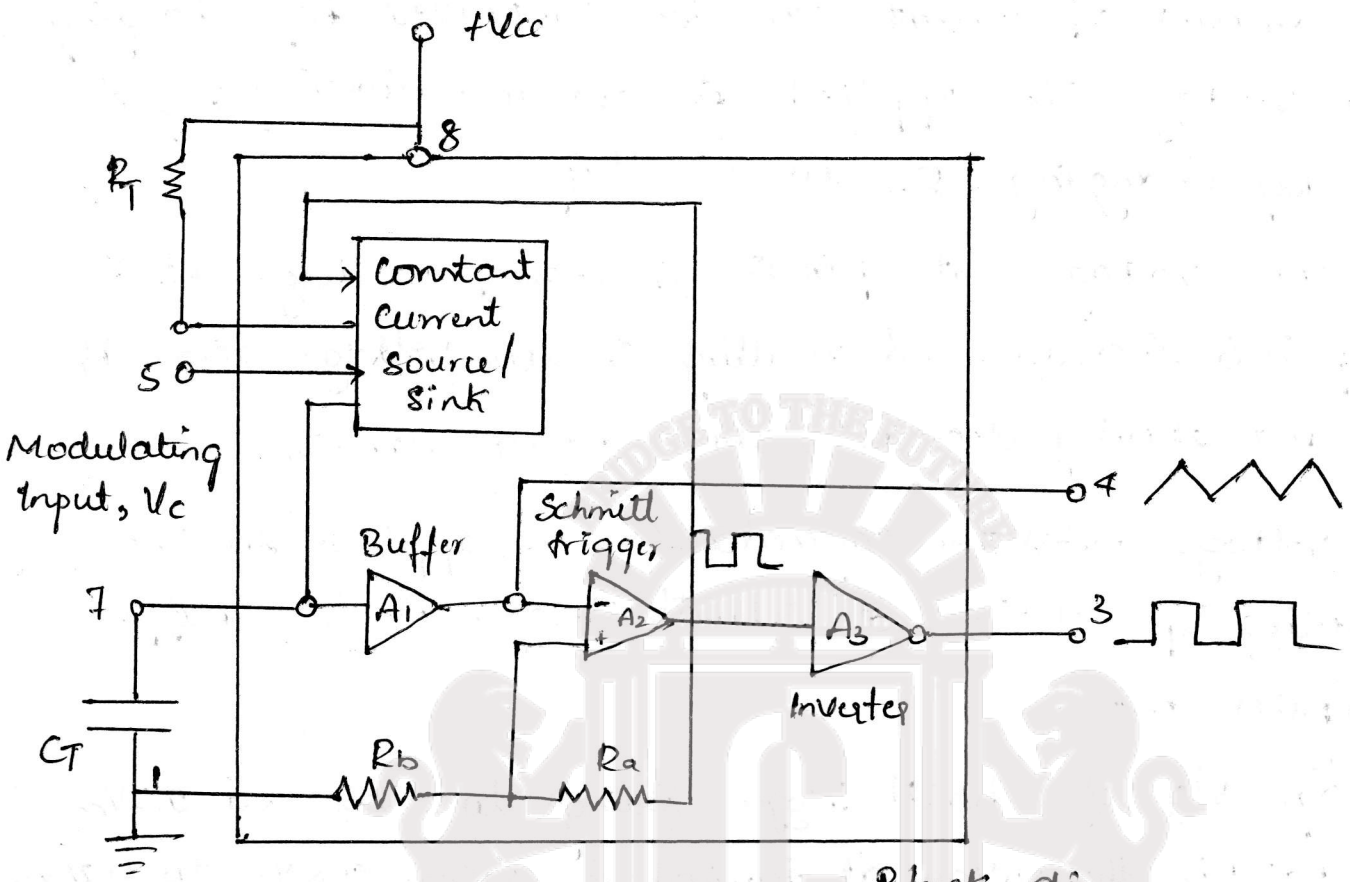
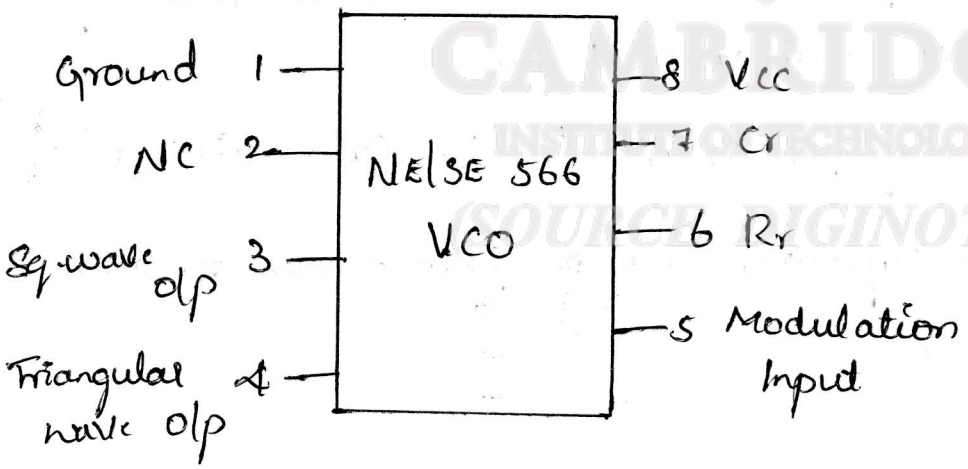


fig (c)

→ Voltage controlled oscillator (VCO):



Block diagram



pin configuration

- A VCO is commonly used in converting low frequency into an audio frequency Range.
- The amount of current can be controlled by changing the voltage V_c applied at the modulating input or by changing R_T to IC chip.
- If the voltage at pin 5 increase, voltage at pin 6 increases and resulting in less voltage across R_T and thereby decreasing the charging current.
- The voltage across the capacitor C_T is applied to the inverting i/p terminal of Schmitt Trigger A_2 via buffer Amplier A_1.
- The o/p v/g of schmitt trigger swings to V_{CC} and $0.5V_{CC}$
- If $R_a = R_b$ the voltage at terminal A_2 swings $0.5V_{CC}$ to $0.25V_{CC}$
- This gives a triangular to voltage waveform at pin 4 and across C_T
- The square wave o/p of the schmitt trigger is inverted by inverter A_3 and is available at pin 3.

<u>The o/p frequency of the VCO can be calculated as</u>:

The total v/g on the capacitor changes from $0.25V_{CC}$ to $0.5V_{CC}$.

So, $$\frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

(or) $$\frac{0.25V_{CC}}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25V_{CC}C_T}{i}.$$

The time period of triangular w/f $= 2\Delta t$.

$$\therefore \quad f_0 = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5 V_{CC} C_T}$$

$$i = \frac{V_{CC} - V_C}{R_T}$$

where V_C is the voltage at pin 5. Therefore.

$$\boxed{f_0 = \frac{2(V_{CC} - V_C)}{C_T R_T V_{CC}}}$$

If the voltage at pin 5 is biased at $\frac{7}{8} V_{CC}$

$$f_0 = \frac{2\left(V_{CC} - \frac{7}{8} V_{CC}\right)}{C_T R_T V_{CC}} = \frac{1}{4 R_T C_T}$$

$$\boxed{f_0 = \frac{0.25}{R_T C_T}}$$

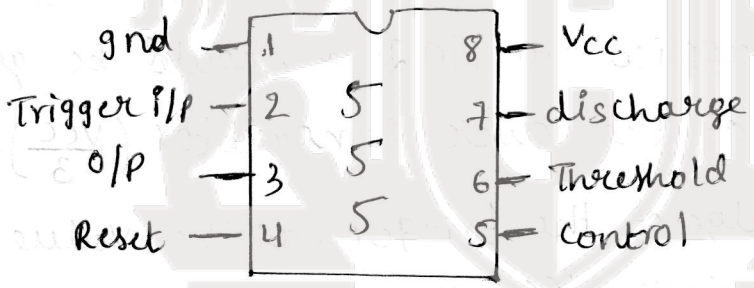
~~Unit - 8~~ Module - 5C

555 - Timers

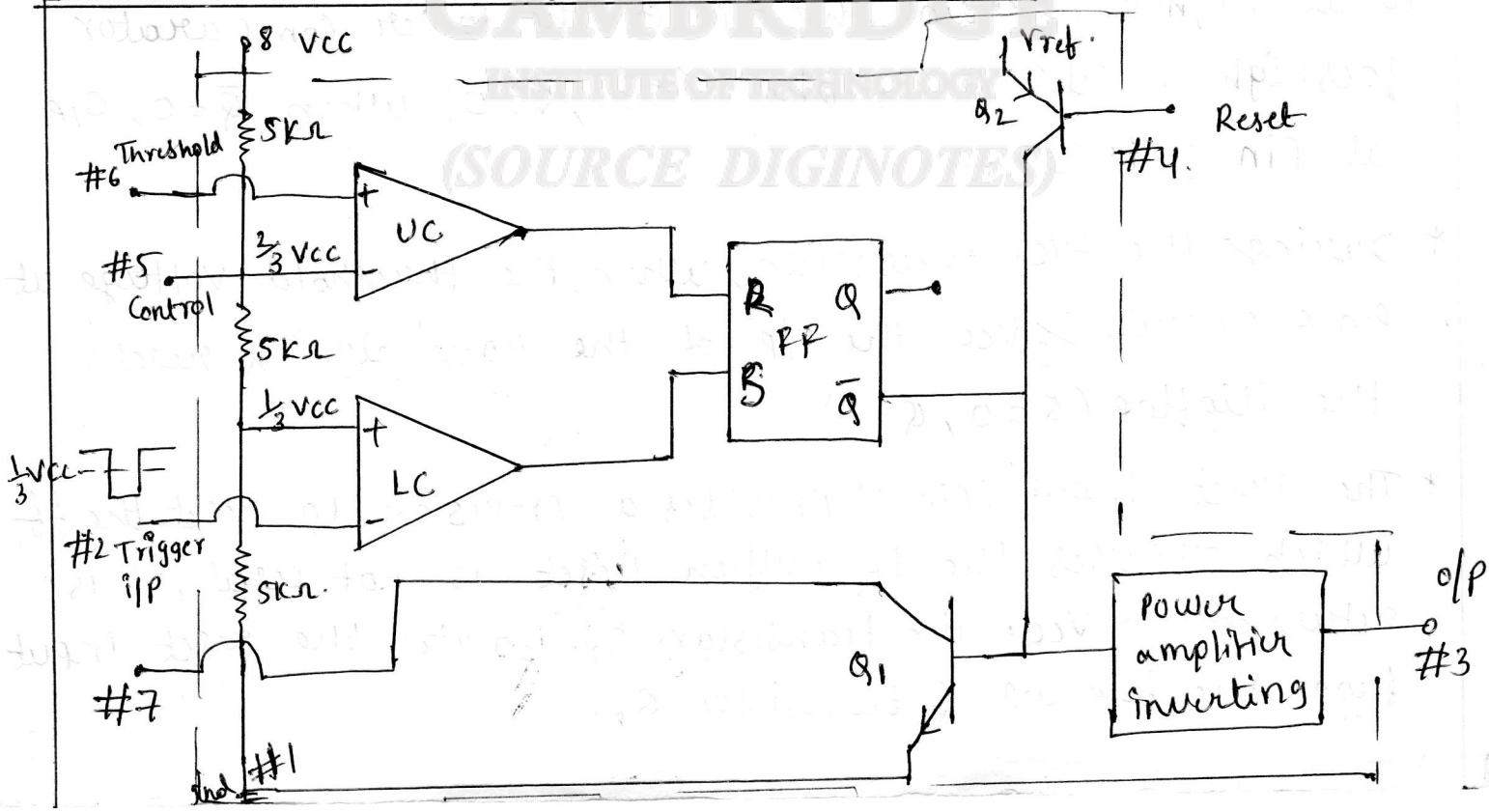
555-Timer :-

* The IC 555 timer is one of the most versatile linear IC. used for Generating accurate time delay or oscillation.
* IC 555 timer is available in two Packages
  (i) 8-pin circular style &
  (ii) 8-pin DIP type.
* IC 555 timer is operated in two modes:
  (i) monostable multivibrator mode &
  (ii) Astable or free running mode.

Pin-Configuration of DIP 555 timer :-



Functional block diagram of 555 timer :-



* The functional diagram shows that 5KΩ internal resistors acts as voltage divider, providing bias voltage of $\frac{2}{3}$ Vcc to the upper comparator (UC) & $\frac{1}{3}$ Vcc to lower comparator (LC). Vcc is the supply voltage.

* These two voltages [i.e $\frac{2}{3}$ Vcc & $\frac{1}{3}$ Vcc] fix the necessary comparator threshold voltage, they also aid in determining the timing interval.

* It can also be varied electronically by applying a modulation voltage to the input terminal no 5 (pin 5: control voltage).

→ In applications, where no such modulation is intended, a capacitor b/w pin 5 & ground is recommended to bypass noise (or) ripple from the supply.

* In stable state the o/p $\bar{Q}$ of the FF is high. This makes the o/p at pin 3 low because power amplifier is a inverter. A -ve going pulse is applied to pin 2 & should be greater than the threshold level of the lower comparator ($\frac{Vcc}{3}$).

* At the -ve going edge of the trigger, as the value of the -ve going edge goes below $\frac{Vcc}{3}$, the non-inverting terminal is at higher potential, the o/p of the lower comparator goes high & sets the flipflop ($Q=1, \bar{Q}=0$) when $\bar{Q}=0$, o/p at pin 3 is high.

* During the +ve excursion, when the threshold voltage at pin 6 exceeds $\frac{2}{3}$ Vcc, the o/p of the goes "high" & resets the flipflop ($Q=0, \bar{Q}=1$)

* The reset input (pin 4) provides a provision to reset the ff which bypasses the ff. When reset is not used, it is returned to Vcc. The transistor Q_2 isolates the reset input from the flipflop & transistor Q_1.

The transistor Q_2 is driven by an internal reference voltage obtained from supply voltage V_{cc}.

mono stable multivibrator :-

Functional block diagram :-

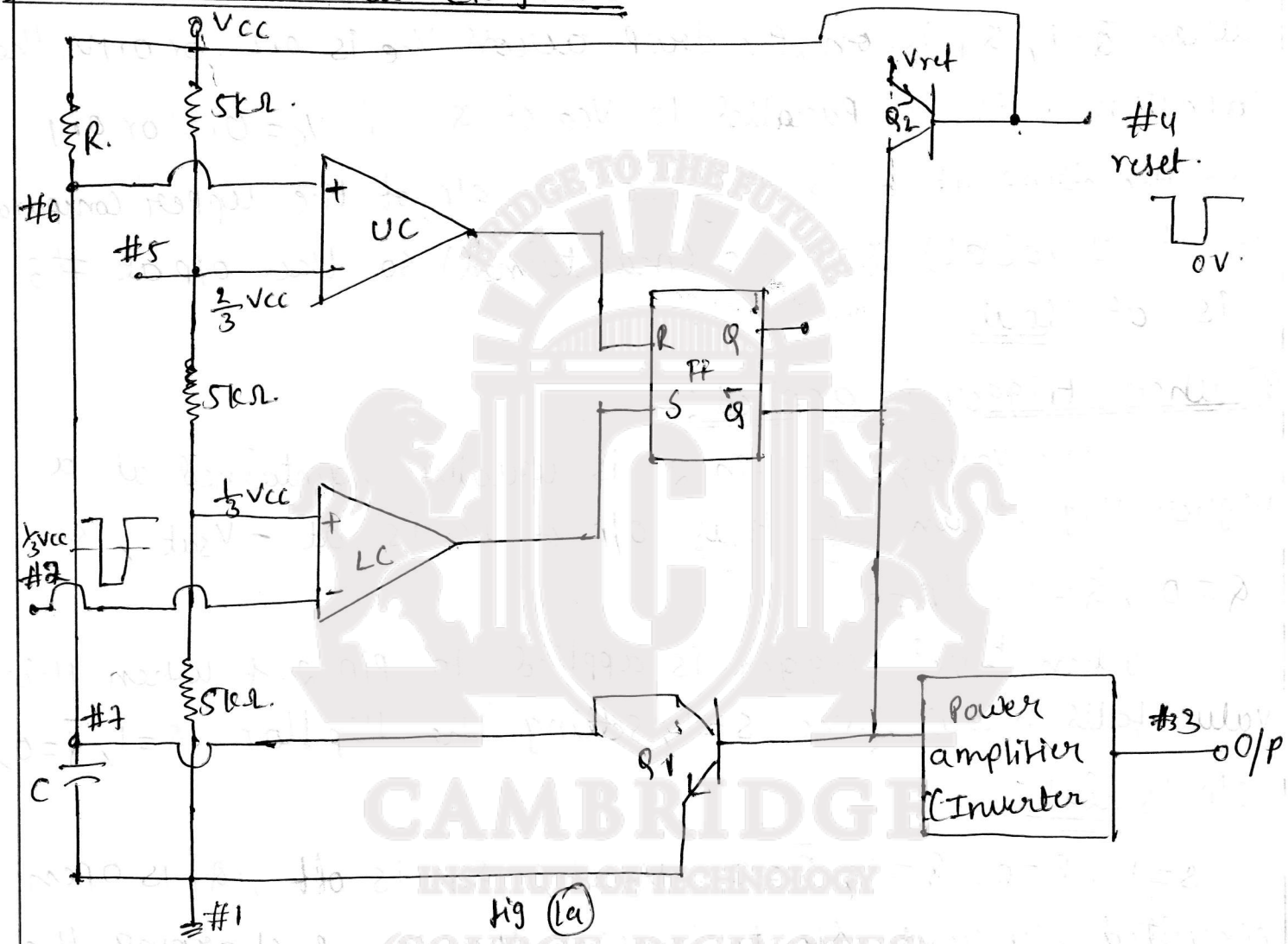


fig (1a)

pin diagram :-

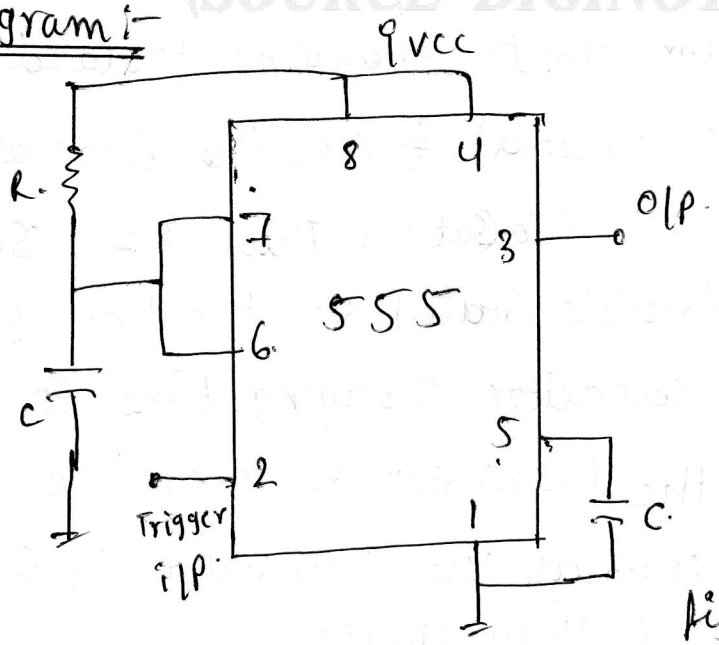


fig (1b)

Fig (1a) & (1b) shows the circuit diagram & functional diagram for monostable operation

In stable state i.e.

(1) Before applying trigger:- $S=0, R=0, Q=0, \bar{Q}=1$.

when $\bar{Q}=1$, Power amplifier is a inverter so o/p is "low"

when $\bar{Q}=1$, Q_1 is on, the drop across V_{ce} is 0.2 or 0.1V, the capacitor C is in parallel to V_{ce} of Q $\therefore V_c = 0.2$ or 0.1

So the drop at 6 is $< \frac{2}{3}V_{cc}$, so o/p of the upper comparator is at $\pm V_o(sat)$ so $R=0$ (maintained) so the o/p at #3 is at low

(2) when trigger is applied:-

The voltage at pin 2 is usually maintained at a higher v/g than $\frac{V_{cc}}{2}$ thus o/p of LC is at $-V_{sat}$, so $Q=0, \bar{Q}=1$, o/p $=0$

when '-ve' trigger is applied to pin 2 & when this value falls below $\frac{1}{3}V_{cc}$ $S=1$, setting the flip flop $Q=1, \bar{Q}=0$, o/p is high

$S=1, R=0, Q=1, \bar{Q}=0, V_o=1$, Q_1 is off, Q_1 is open circuited, current starts flowing through R charging the capacitor, the capacitor starts charging towards V_{cc}, but when the V_c reaches (exceeds) $\frac{2}{3}V_{cc}$, the drop at 6 is higher, that o/p of UC is at $+V_o(sat)$. Thus $R=1$, so $Q=0$, $\bar{Q}=1$, o/p is low (stable state) so the time for which o/p is high is the capacitor charging time to a value of $\frac{2}{3}V_{cc}$. when $\bar{Q}=1$, the transistor Q_1 is on, so the capacitor starts discharging through the transistor Q_2 & the discharge time is very short.

Problems :

1] Design a monostable multivibrator using 555 timer to obtain a pulse width of 10msec **Jan-10, 6M**

Sol: Given, $T = 10msec$.

WKT, $T = 1.1 R_A C$

$$R_A C = \frac{T}{1.1}$$

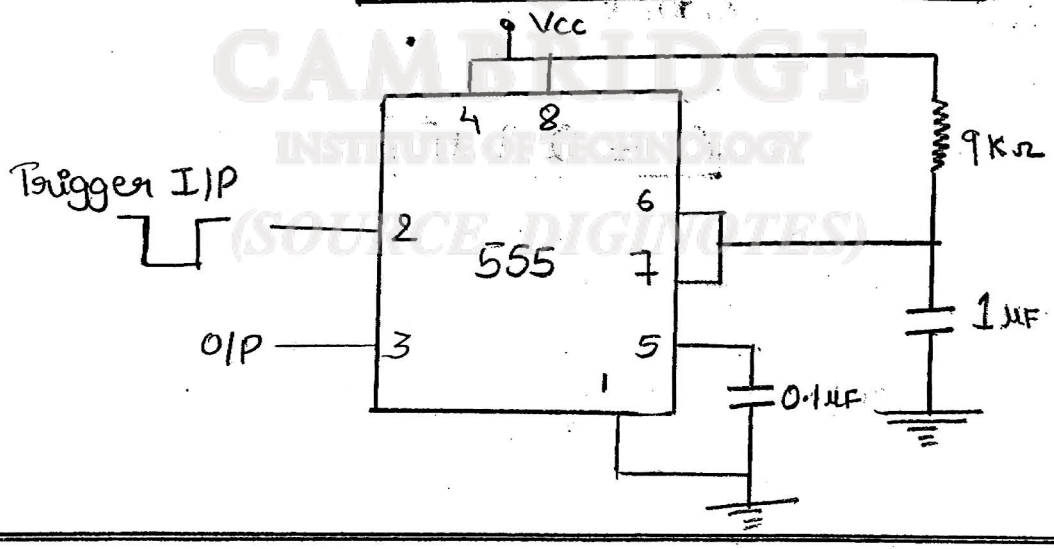
$$R_A C = \frac{10 msec}{1.1}$$

$$R_A C = 9.09 msec$$ ← 1M

Assume $C = 1 \mu F$ ← 1M

$$R_A = \frac{9.09 msec}{1 \mu F} = 9.09 k\Omega$$

$\therefore$ $R_A = 9.9 k\Omega$ ← 2M



2] In the monostable multivibrator, the Component values are $R_A = 5.6K\Omega$, $C = 0.068\mu F$. Find the pulse width T.

Sol:- WKT, $T = 1.1 R_A C$

$= 1.1 \times 5.6K\Omega \times 0.068\mu F$

$\boxed{T = 0.42 msec}$

3] In the monostable multivibrator, $R = 100K\Omega$ & the time delay $T = 100msec$. Calculate the value of C. Verify the value of C obtained.

Sol:- WKT,

$T = 1.1 R_A C$

$T = 1.1 \times 100K\Omega \times C$

$\frac{100msec}{1.1 \times 100K\Omega} = C$

$\boxed{C = 0.9\mu F}$

The capacitor voltage is given by

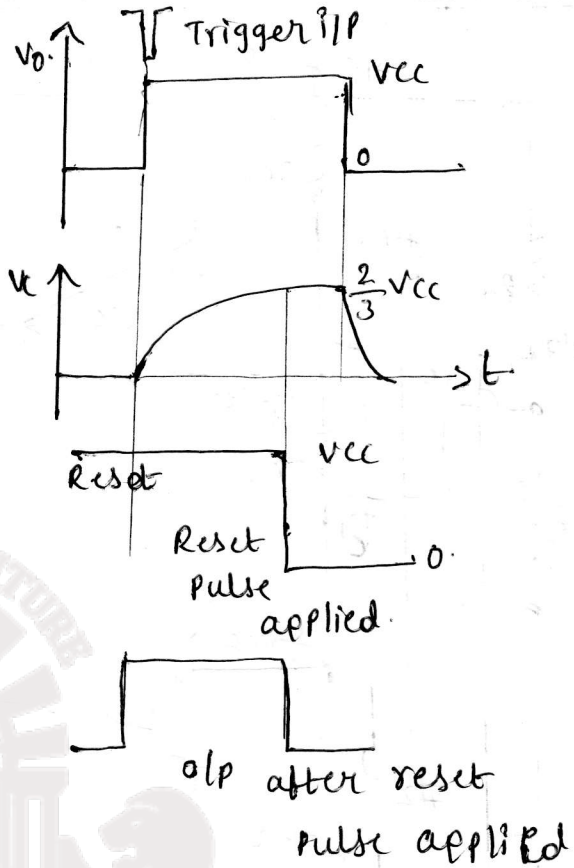
$$V_c = V_f + (V_i - V_f)e^{-t/\tau}$$

$V_c \rightarrow$ capacitor voltage

$V_f \rightarrow$ final voltage

$V_i \rightarrow$ Initial voltage

τ - Time constant RC.



At $0 < t < T_p$

$V_i = V_c(t=0) = 0V$

$V_f = V_c(t \rightarrow \infty) = V_{cc}$

$\tau = RC$

$V_c = V_{cc} + (0 - V_{cc})e^{-t/RC}$

$V_c = V_{cc} - V_{cc}e^{-t/RC} \rightarrow (1)$

At $t = t_p \Rightarrow V_c = \frac{2}{3}V_{cc}$

$V_c = V_{cc} - V_{cc}e^{-t_p/RC}$

$\frac{2}{3}\cancel{V_{cc}} = \cancel{V_{cc}}(1 - e^{-t_p/RC})$

$\frac{2}{3} = 1 - e^{-t_p/RC}$

$e^{-t_p/RC} = 1 - 2/3$

$e^{-T_p/RC} = 1/3$

$\frac{1}{e^{T_p/RC}} = \frac{1}{3}$ $[T_p = t_{on}]$

$e^{T_p/RC} = 3$

$\ln e^{T_p/RC} = \ln 3$

$$\boxed{T_p = 1.1RC}$$

$$\boxed{T_{on} = 1.1RC}$$

555 timer used as astable multivibrator:-

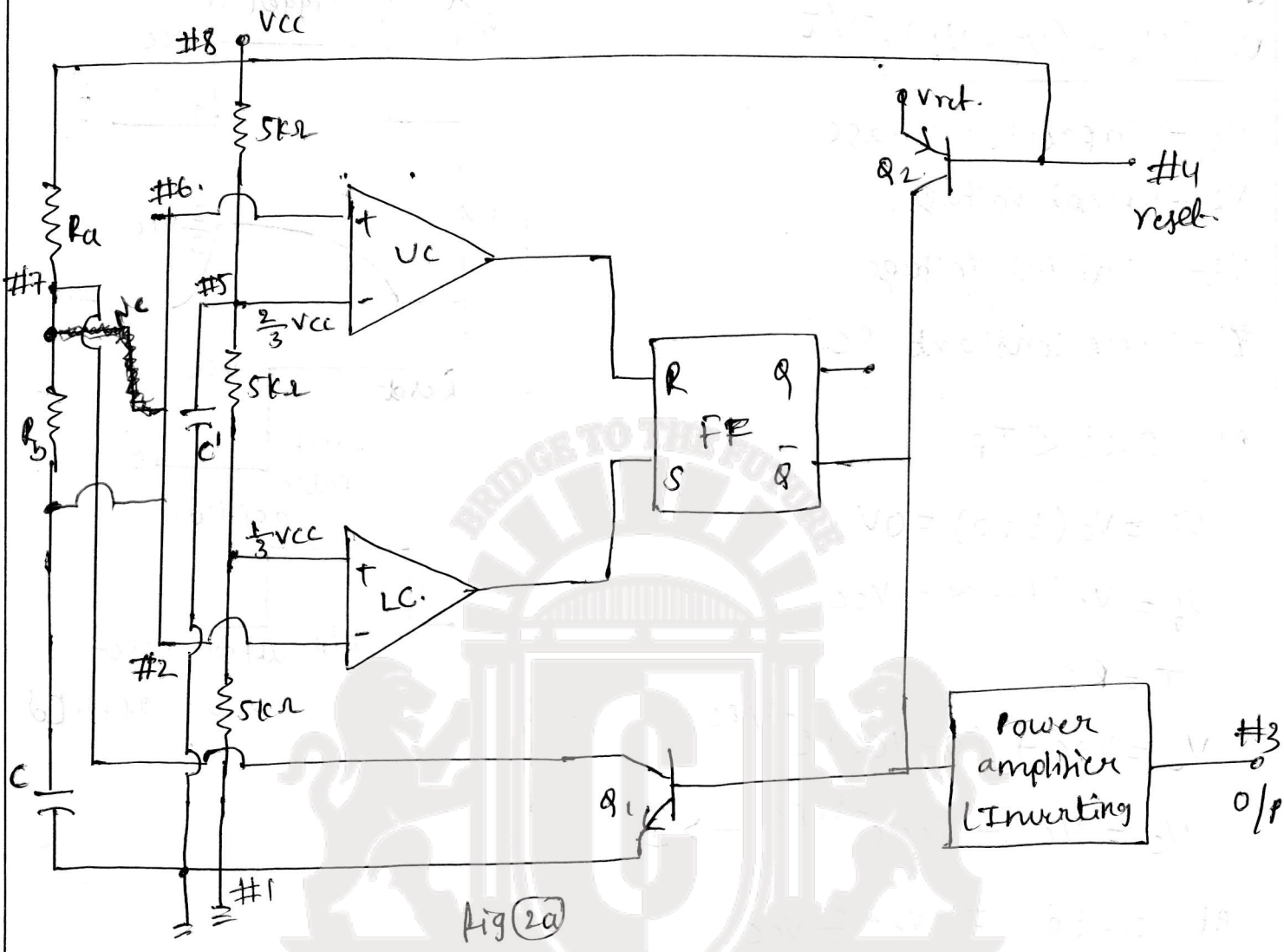


fig (2a)

Pin Diagram:-

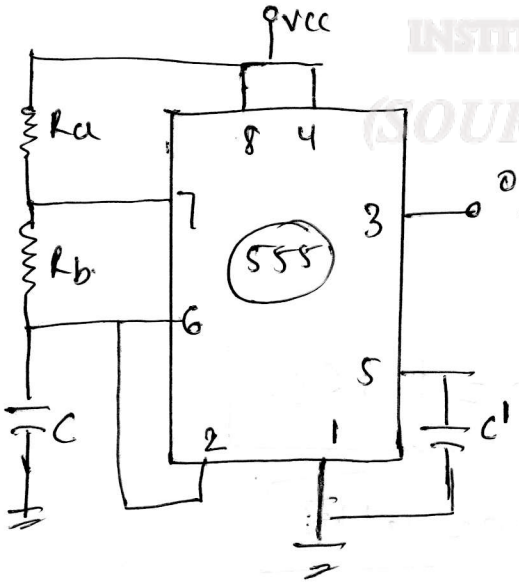


fig (2b)

Fig (2b) & (2a) shows the IC 555 connected as an astable multivibrator

* The threshold i/p (pin no. 6) is connected to the trigger i/p.
* Two external resistors Ra, Rb & a capacitor C is used as shown.
* This circuit has "no stable state" & changes its state alternatively. Hence the operation is also free running non-sinusoidal oscillator

① When power supply is switched on

current flows from V_{cc} towards ground, drop at pin 5 is at $\frac{2}{3}V_{cc}$ & 2c has a drop of $\frac{1}{3}V_{cc}$.

$\therefore S=1, R=0, Q=1, \bar{Q}=0, V_0=1$, Q_1 is off

Capacitor starts charging towards V_{cc} with time constant $(R_a+R_b)C$

② when V_c (voltage across capacitor) exceeds $\frac{1}{3}V_{cc}$.

$\underbrace{S=0, R=0}_{\text{Previous condition.}}, Q=1, \bar{Q}=0, V_0=1$, Q_1 is off.

Capacitor continuous to charge towards V_{cc}.

③ when V_c exceeds $\frac{2}{3}V_{cc}$

$S=0, R=1, Q=0, \bar{Q}=1, V_0=0$, Q_1 is on

Q_1 is on $\Rightarrow$ capacitor starts to discharge with time constant RC

④ when V_c falls below $2/3\,V_{cc}$

$S=0, R=0$ (previous), $Q=0, \bar{Q}=1, V_0=0$, Q_1 is on

Q_1 is on $\Rightarrow$ Capacitor continues to discharge towards zero.

⑤ when V_c falls below $1/3\,V_{cc}$.

$S=1, R=0, Q=1, \bar{Q}=0$, Q_1 is off, V_0 = high

Q_1 off $\Rightarrow$ Capacitor starts to charge again towards V_{cc} with time constant $(R_a+R_b)C$.

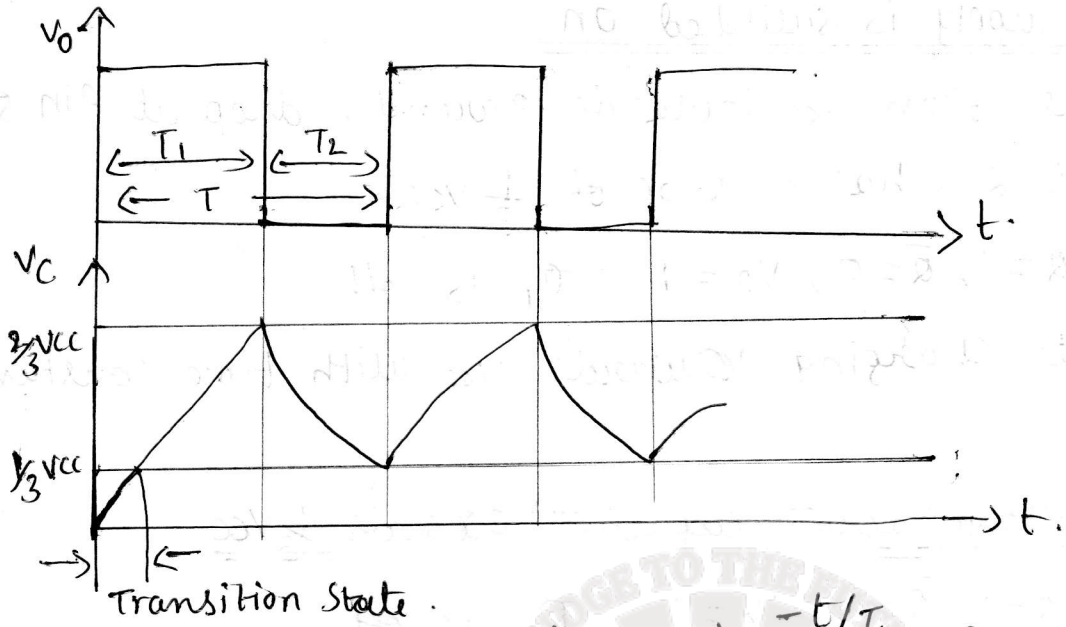
⑥ when V_c exceeds $1/3\,V_{cc}$.

$S=0, R=0, Q=1, \bar{Q}=0, V_0=1$, Q_1 is off, which is cond^n ②

Thus the cycle repeats i.e from ② to ⑤ thus generating a square wave

when capacitor is charging o/p is high

discharging o/p is low.



$0 < t < T \qquad V_C = V_f + (V_i - V_f)e^{-t/\tau} \rightarrow (1)$

$V_i = V_C(t=0) = \frac{1}{3}V_{CC}$

$V_f = V_C(t=\infty) = V_{CC}$

Expression for charging time of capacitor on period of a stable multivibrator.

$$V_C = V_{CC} + \left(\frac{1}{3}V_{CC} - V_{CC}\right)e^{-t/\tau_{charging}}$$

$$V_C = V_{CC} - \frac{2}{3}V_{CC}\, e^{-t/\tau_{charging}}$$

$$V_C = V_{CC}\left(1 - \frac{2}{3}e^{-t/\tau_{charging}}\right) \rightarrow (2)$$

At $t = t_{on}$, $V_C = \frac{2}{3}V_{CC}$. In eq^n (2) $\Rightarrow$

$$\frac{2}{3}\cancel{V_{CC}} = \cancel{V_{CC}}\left(1 - \frac{2}{3}e^{-t_{on}/\tau_{charging}}\right).$$

$$\frac{2}{3}e^{-\frac{T_{on}}{\tau_{charging}}} = 1 - \frac{2}{3}$$

$$e^{-\frac{T_{on}}{\tau_{charging}}} = \frac{1}{\cancel{3}} \times \frac{\cancel{3}}{2}$$

$$\frac{1}{e^{\frac{T_{on}}{\tau_{charging}}}} = \frac{1}{2}$$

$$e^{\frac{T_{on}}{\tau_{charging}}} = 2$$

Taking ln on both sides, we get

$$\frac{T_{on}}{\tau_{charging}} = \ln(2)$$

$$T_{on} = 0.693\ \tau_{charging}$$

where,
$\tau_{charging} = (R_A + R_B)\,C$

$$\boxed{T_{on} = 0.693\,(R_A + R_B)C} \rightarrow (A)$$

Expression for discharging time of capacitor on period of astable multivibrator.

$$V_c = V_f + (V_i - V_f)\,e^{-t/\tau_{discharging}}$$

$\tau_{discharging} = R_B C$

$$V_i = V_c\ (\text{at } t = 0^+) = \frac{2}{3}V_{CC}$$

$$V_f = V_c\ (\text{at } t = \infty) = 0V$$

$$V_c = 0 + \left(\frac{2}{3}V_{CC} - 0\right) e^{-t/\tau_{discharging}}$$

$$V_c = \frac{2}{3}V_{CC}\, e^{-t/\tau_{discharging}} \rightarrow (2)$$

At $t = t_{off}$; $V_c = \frac{1}{3}V_{CC}$ in eq^n (2)

$$\frac{1}{\cancel{3}}\cancel{V_{CC}} = \frac{2}{\cancel{3}}\cancel{V_{CC}}\, e^{\frac{-t_{off}}{\tau_{discharging}}}$$

$$e^{\frac{-t_{off}}{\tau_{discharging}}} = \frac{1}{2}$$

$$\frac{1}{e^{\frac{t_{off}}{\tau_{discharging}}}} = \frac{1}{2}$$

$$e^{\frac{t_{off}}{\tau_{discharging}}} = 2$$

Taking ln on both sides

$$\frac{T_{off}}{\tau_{discharging}} = 0.693$$

$$\boxed{T_{off} = 0.693\, R_B\, C} \rightarrow (B)$$

A free-running oscillations/frequency is given by

$f = \frac{1}{T}$ where T = Period of one complete cycle

$f = \frac{1}{T}$ $T = T_{on} + T_{off}$

$T = 0.693(R_A + R_B)C + 0.693 R_B C$

$f = \frac{1}{0.693(R_A + 2R_B)C}$

$$\boxed{f = \frac{1.45}{(R_A + 2R_B)C}}$$

PROBLEM:-

① A 555 timer has a stable multivibrator $R_A = 2.2k\Omega$, $R_B = 6.8k\Omega$ & $C = 0.01\mu F$. Calculate (i) T_{high} (ii) T_{low} (iii) Free-running frequency (iv) Duty-cycle

(i) $T_{high} = 0.693(R_A + R_B)C$

$= 0.693(2.2k + 6.8k) \times 0.01\mu$ $\boxed{T_{high} = 62.37\,\mu sec}$

(ii) $T_{low} = 0.693 R_B C$

$= 0.693(6.8k)(0.01\mu)$ $\boxed{T_{low} = 47.12\,\mu sec}$

(iii) $f = \frac{1.45}{(R_A + 2R_B)C}$

$= \frac{1.45}{(2.2k + 2 \times 6.8k) \times 0.01\mu}$ $\boxed{f = 9.114\,KHz}$

(iv) Duty cycle $= \frac{T_{on}}{T_{on} + T_{off}}$

$= \frac{62.37\mu}{62.37\mu + 47.12\mu}$ $\boxed{\text{Duty cycle} = 56.96\%}$

Duty cycle:-

Generally the charging time constant is greater than the discharging time constant. Hence at the o/p, the wave form is not symmetric. The ratio of high o/p period and low o/p period is given by a mathematical parameter called Duty cycle

$$\text{Duty cycle} = \frac{\text{high output}}{\text{Total time of one cycle}}$$

$W = T_{on} \rightarrow$ Time for o/p is high

$T \rightarrow$ Time of one cycle

$$\text{Duty} = \frac{W}{T} = \frac{T_{on}}{T_{on} + T_{off}}$$

$$\% \text{ Duty cycle} = \frac{T_{high}}{T} \times 100$$

$$= \frac{\cancel{0.69}(R_A + R_B)\cancel{C}}{\cancel{0.69}(R_A + 2R_B)\cancel{C}} \times 100$$

$$\boxed{\% \text{ Duty cycle} = \frac{R_A + R_B}{R_A + 2R_B} \times 100.}$$

Eg:- Design an astable multivibrator to have a duty cycle of 70%.

Sol^n:- duty cycle $= \frac{R_A + R_B}{R_A + 2R_B} \times 100$

$$70 = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

$$7R_A + 14R_B = 10R_A + 10R_B.$$

$$3R_A = 4R_B$$

$$\boxed{R_A = \frac{4}{3} R_B.}$$

For 50% duty cycle

$$50 = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

$5R_A + 10R_B = 10R_A + 10R_B$.

$1 = 2$ ⇒ This is not possible, so a stable multivibrator cannot be designed for duty cycle ≤ 50%.

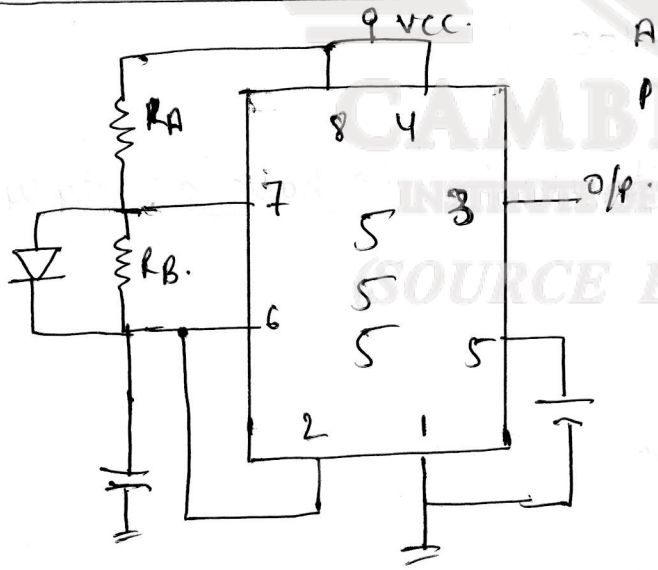
It can be designed only for duty cycle above 50%.

[logically $(R_A + R_B)C > R_B C$ ∴ on time is always greater than off time so 50% duty cycle is not possible].

An a stable multivibrator can also be designed to give a duty cycle of 50% less by just connecting a diode in parallel with R_B.

The duty cycle can be made approach 50% by selecting $R_B >> R_A$.

To Get symmetric wave-form:-

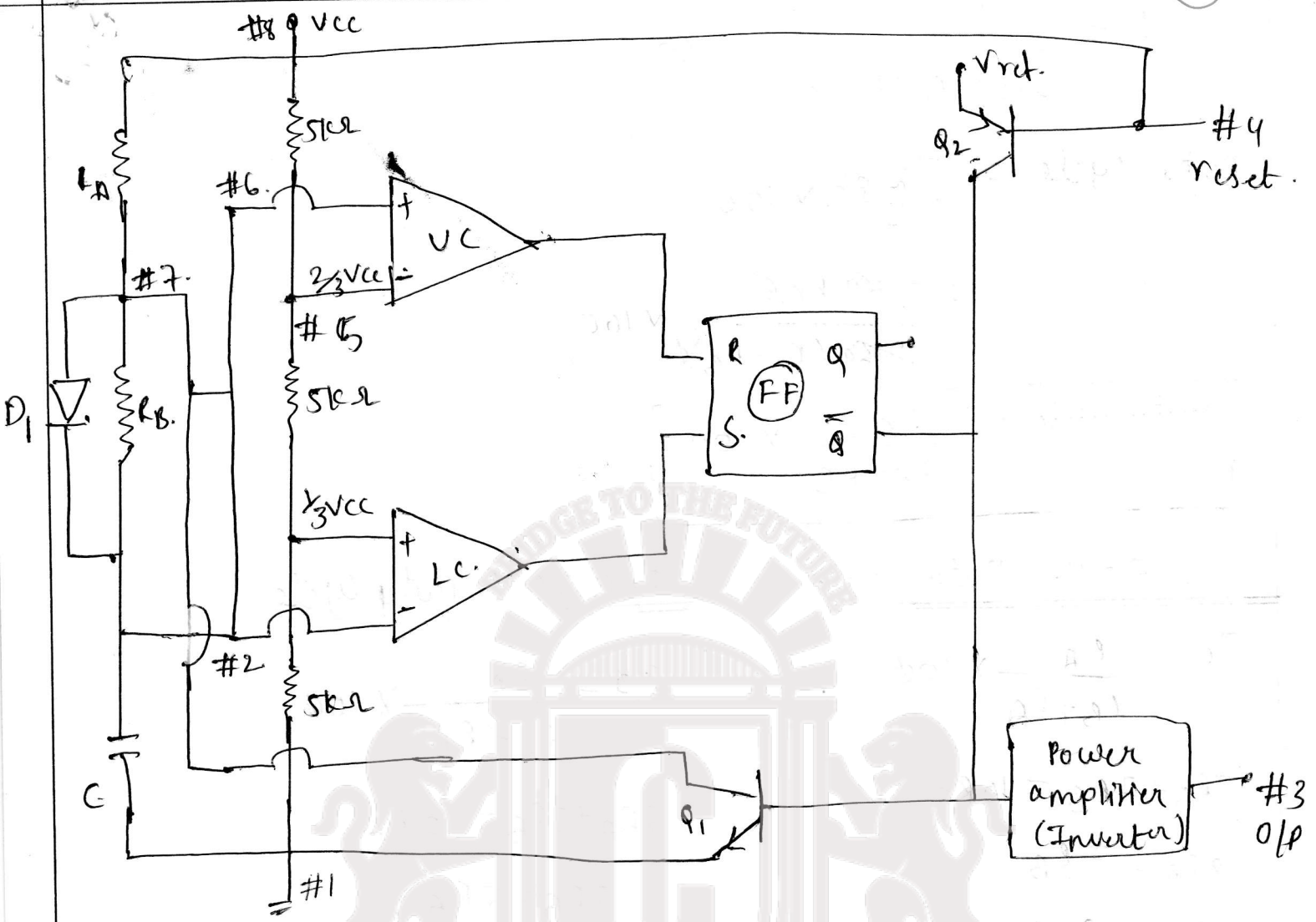


A duty cycle of 50% or less can be produced by including diode D_1 in the circuit as illustrated in fig

In this arrangement resistor R_B is by-passed during the charging time of C, as the charging current flows through R_A & diode D_1.

During the discharge time, D_1 is reverse biased, the discharge current flows from C_1 via R_B to terminal 7.

If resistors R_A & R_B are equal, the charge & discharge times will be close.



when power is turned on the current starts flowing through R_A, D_1 & C_1 [since diode is forward biased], so that the time constant $\tau_c = R_A \cdot C$.

when $V_C > \frac{2}{3} V_{cc}$, Q_1 - on, V_o - low $Q_2 \rightarrow$ on, capacitor starts to discharge. now diode is reverse biased, the current flows through R_B & transistor.

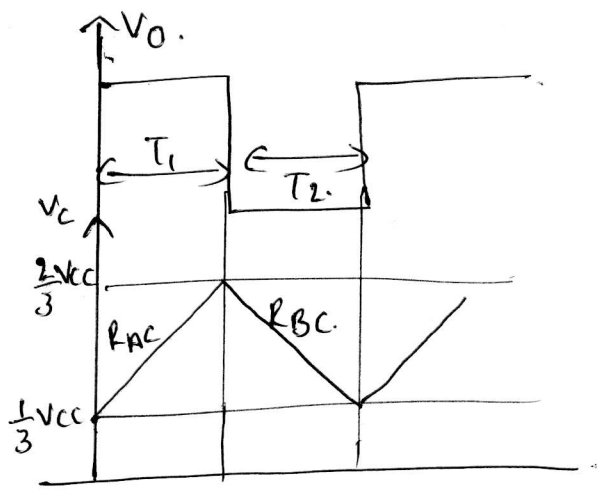
$\tau_d = R_B \times C$.

$\therefore T_1 = 0.69 R_A C \rightarrow (1)$

$T_2 = 0.69 R_B C \rightarrow (2)$

$T = T_1 + T_2$

$T = 0.69 (R_A + R_B) C \rightarrow (3)$



$$f = \frac{1}{0.69(R_A+R_B)C} \rightarrow (A)$$

$$\text{Duty cycle} = \frac{T_{high}}{T} \times 100$$

$$= \frac{\cancel{0.69} R_A \cancel{C}}{\cancel{0.69}(R_A+R_B)\cancel{C}} \times 100$$

$$\boxed{\text{Duty cycle} = \frac{R_A}{R_A+R_B} \times 100}$$

For 70% Duty cycle

$$70 = \frac{R_A}{R_B+R_A} \times 100$$

$$7R_A + 7R_B = 10R_A$$

$$3R_A = 7R_B$$

$$R_A = \frac{7}{3} R_B$$

$$R_B = \frac{3}{7} R_A.$$

$$\boxed{R_A > R_B}$$

For 50% Duty cycle

$$50 = \frac{R_A}{R_A+R_B} \times 100$$

$$5R_A + 5R_B = 10R_A$$

$$5R_B = 5R_A$$

$$\boxed{R_A = R_B} \rightarrow \text{Possible.}$$

For 20% Duty cycle

$$20 = \frac{R_A}{R_A+R_B} \times 100$$

$$2R_A + 2R_B = 10R_A$$

$$2R_B = 8R_A$$

$$R_B = 4R_A.$$

$$\boxed{R_B > R_A.} \rightarrow \text{Possible.}$$

555 - TIMERS (Not included in syllabus)

* SCHMITT TRIGGER

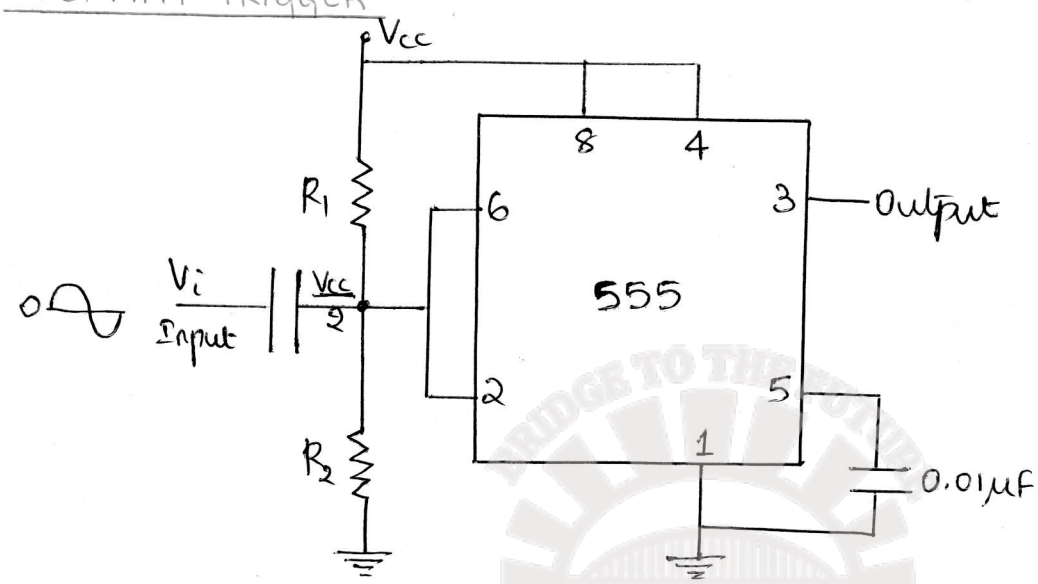
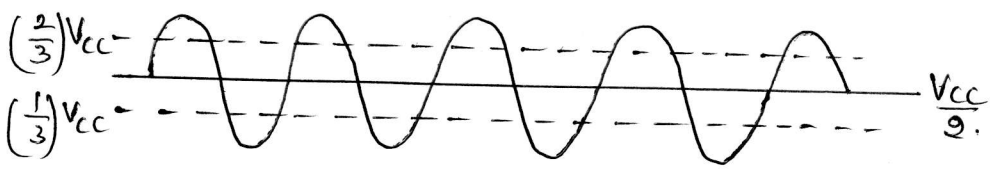


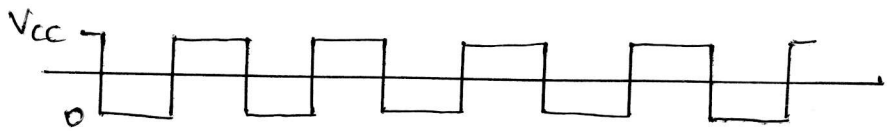
fig: Timer in Schmitt Trigger Operation.

→ The use of 555 timer as a Schmitt trigger is shown in figure. Here the two internal comparators are tied together and externally biased at $V_{cc}/2$ through R_1 and R_2. Since

→ Since the upper comparator will trip at $(2/3)V_{cc}$ and lower comparator at $(1/3)V_{cc}$, the bias provided by R_1 and R_2 is centered within these two thresholds.

→ Thus a sine wave of sufficient amplitude $\left(> \frac{V_{cc}}{6} = \frac{2}{3}V_{cc} - \frac{V_{cc}}{2}\right)$ to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave o/p as shown.

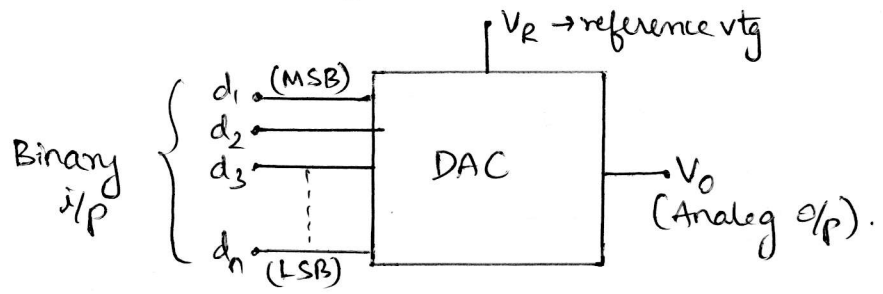




→ It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains same as that of input signal.

MODULE - 5B

* Digital to Analog Converters [DAC]



* The schematic of a DAC is shown in fig. It has an n-bit binary input (d_n), a reference voltage (V_R) to give the analog output signal.
* The output can be voltage or current. The output voltage is generally given by:

$$V_0 = K \times V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right]$$

where, V_0 = output voltage.

V_{FS} = full scale output voltage.

k = scaling factor, usually adjusted to unity (1).

$d_1 d_2 \cdots d_n$ = n-bit binary input.

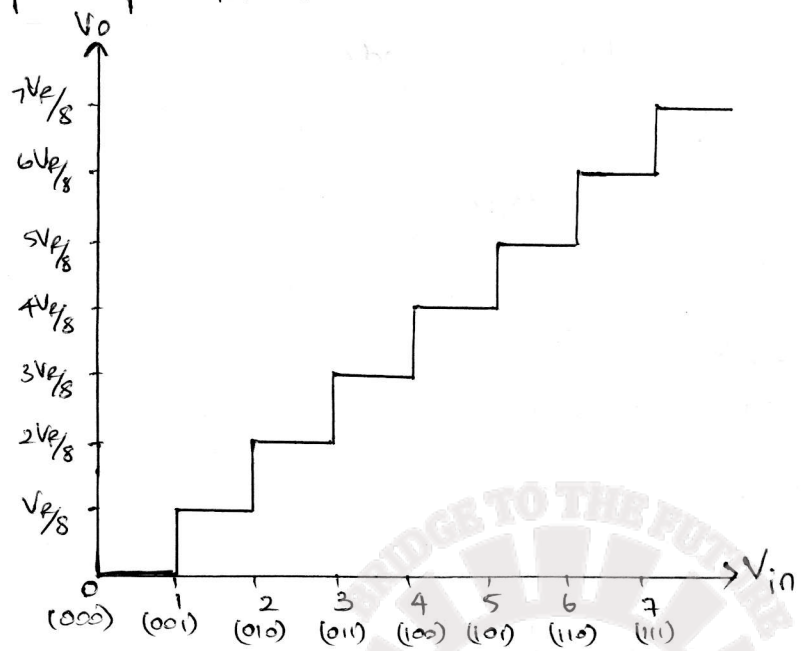
d_1 = most significant bit with a weight of $V_{FS}/2$.

d_n = least significant bit with a weight of $V_{FS}/2^n$.

for 3 input DAC:

I/p's d_1	d_2	d_3	If $V_R = 8$. $V_0 = KV_R[2^{-1}d_1 + 2^{-2}d_2 + 2^{-3}d_3]$	
0	0	0	0	
0	0	1	1	$V_R/8$
0	1	0	2	$2V_R/8$
0	1	1	3	$3V_R/8$
1	0	0	4	$4V_R/8$
1	0	1	5	$5V_R/8$
1	1	0	6	$6V_R/8$
1	1	1	7	$7V_R/8$

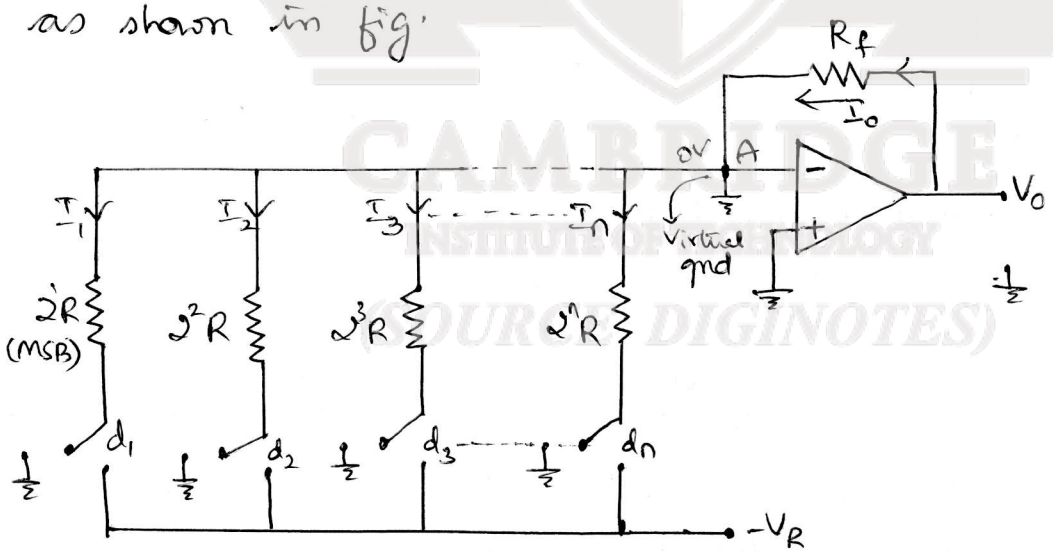
A graph of V_{in} V/s V_o is shown below



Types of DAC :-

1) Weighted Resistor DAC X ← Not included in syllabus
2) R-2R ladder type DAC ← [Included in syllabus]
3) Inverted R-2R ladder. X ← Not included in syllabus.

1) Weighted Resistor DAC :- The circuit of weighted resistor DAC is as shown in fig.



The resistors are in geometric progression. Since an inverting amplifier configuration is used, inverting terminal is at virtual gnd

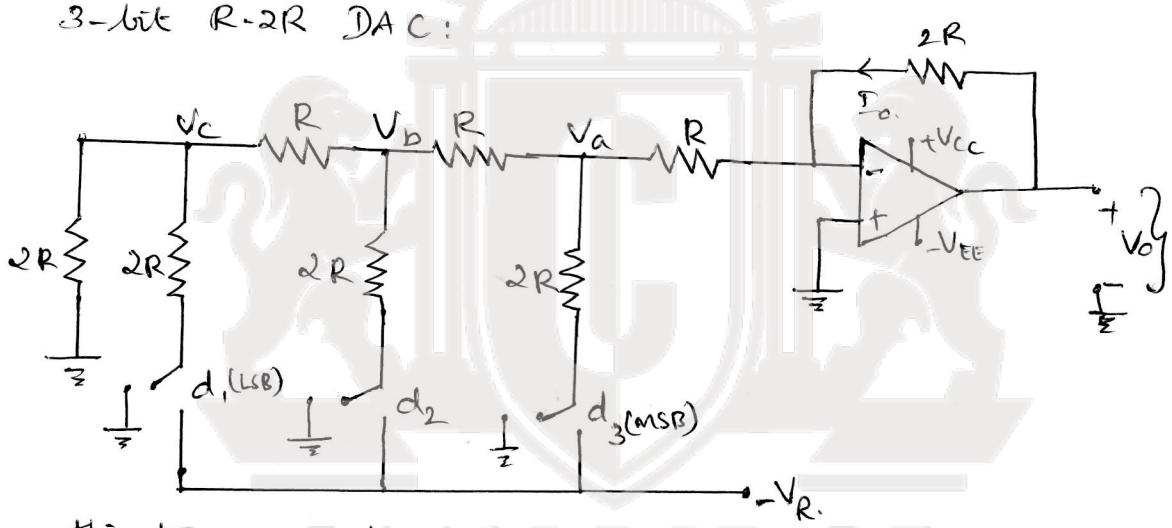
* The weighted resistor network has n-electronic switches $d_1, d_2, \cdots d_n$ controlled by binary input. If the binary i/p to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$).

2) R-2R ladder Type DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5kΩ to 10kΩ.

For simplicity, consider a 3-bit DAC as shown in fig. where the switch position $d_1 d_2 d_3$ corresponds to the binary 100. The circuit can be simplified to the equivalent form of fig. Then, voltage at node C can be easily calculated by the set procedure of network analysis.

3-bit R-2R DAC:



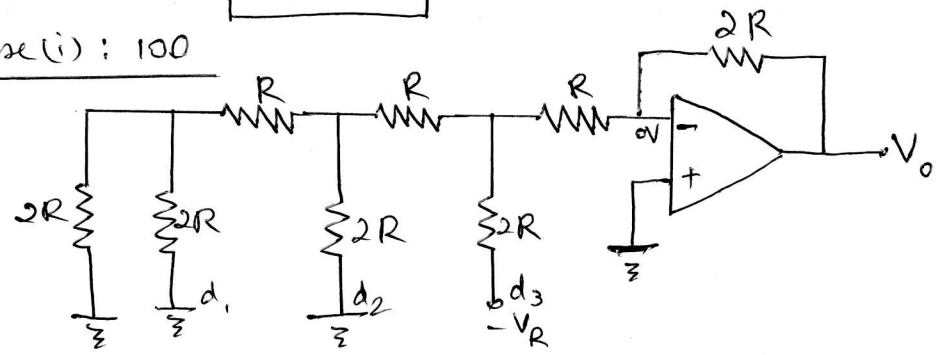
In this type we take for few combinations and solve the rest by using super position theorem. Since inverting amplifier is used

$$V_0 = -\frac{R_f}{R} \cdot V_a$$

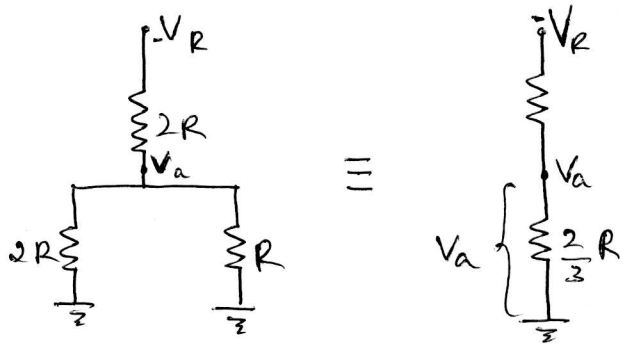
$$= -\frac{2\cancel{R}}{\cancel{R}} \cdot V_a \quad (\because R_f = 2R)$$

$$\boxed{V_0 = -2V_a}$$

Case (i) : 100



To determine V_a



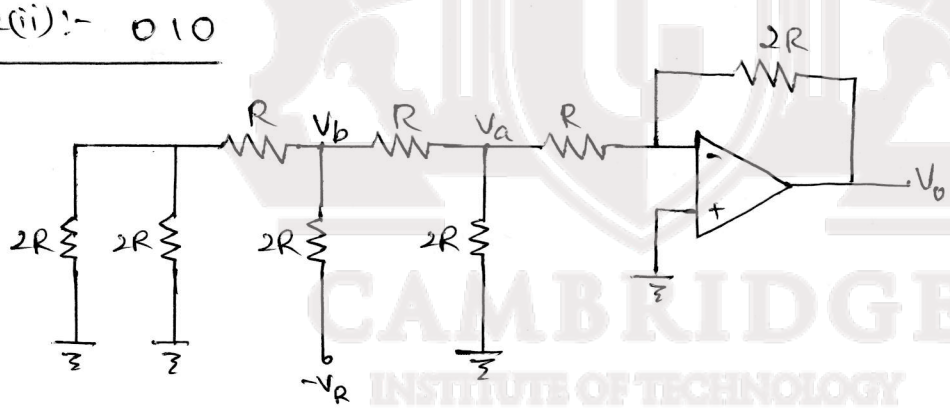
By using voltage divider rule: $V_a = \dfrac{-V_R\left(\frac{2R}{3}\right)}{2R + \frac{2R}{3}} = \dfrac{-\frac{2V_R R}{3}}{\frac{6R+2R}{3}}$

$$V_a = \frac{-2V_R R}{-8R} = \frac{-V_R R}{4R} \qquad \boxed{V_a = -\frac{V_R}{4}}$$

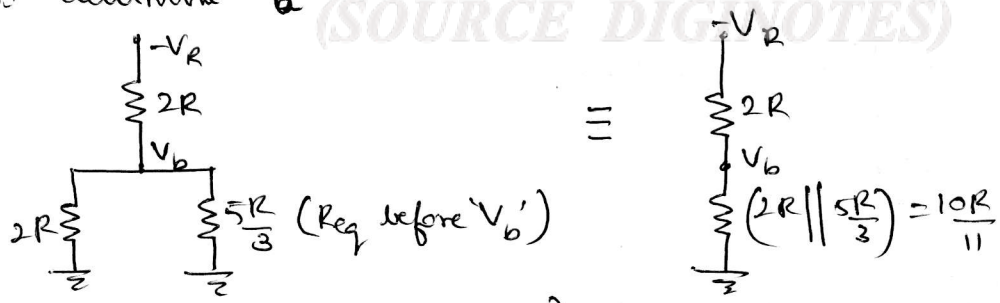
now we have, $V_o = -2V_a \Rightarrow -2\left(\frac{-V_R}{4}\right) = \frac{V_R}{2}$

In general, $\therefore \boxed{V_o = \frac{4V_R}{8}}$

Case(ii):- 010

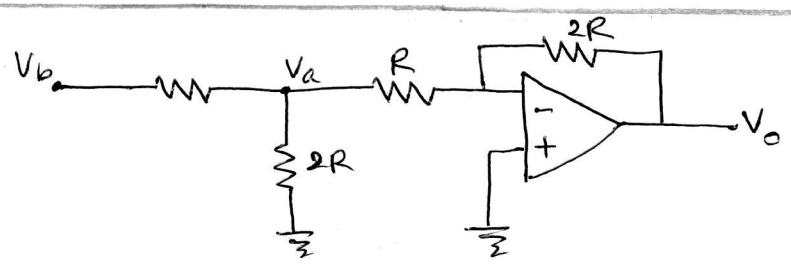


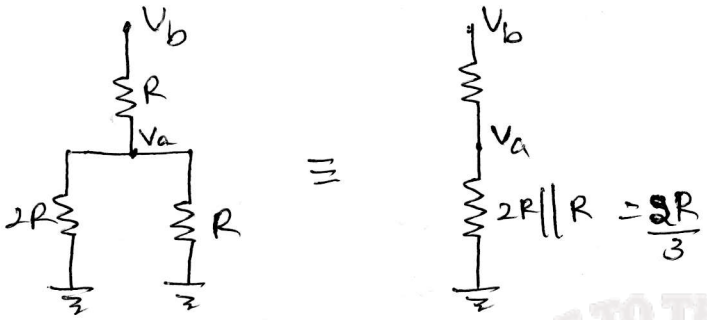
To determine V_b



$$V_b = \frac{-V_R\left(\frac{10R}{11}\right)}{\frac{10R}{11} + 2R} \quad (\because \text{voltage divider rule})$$

$$\boxed{V_b = \frac{-10V_R}{32}}$$





$$V_a = \frac{V_b \frac{2R}{3}}{\frac{2R}{3} + R} = \frac{\left(\frac{-10V_R}{\cancel{32}\,16}\right)\left(\frac{\cancel{2}R}{3}\right)}{\frac{2R}{3} + R} \qquad \left(\because V_b = \frac{-10V_R}{32}\right)$$

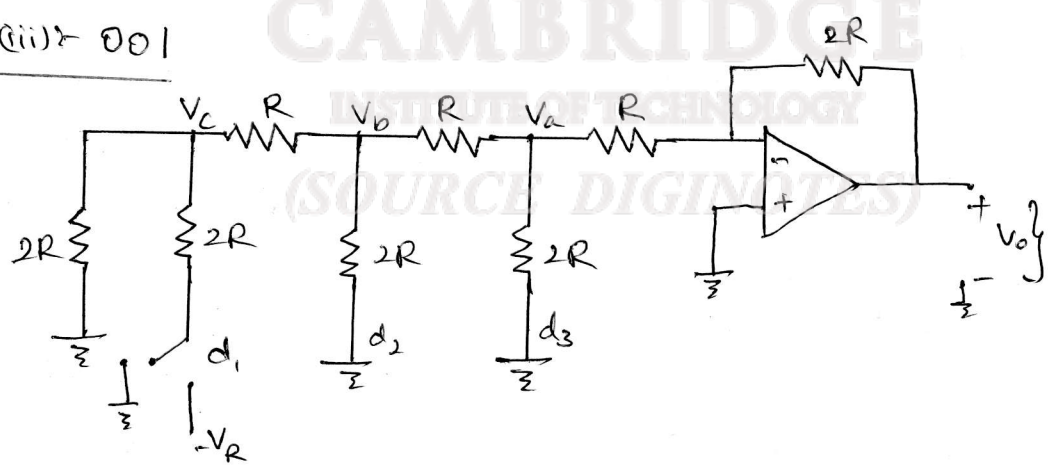
$$V_a = \frac{\frac{-10V_R R}{48}}{\frac{2R+3R}{3}} \qquad \therefore \boxed{V_a = -\frac{V_R}{8}}$$

now we have, $V_o = -2V_a$

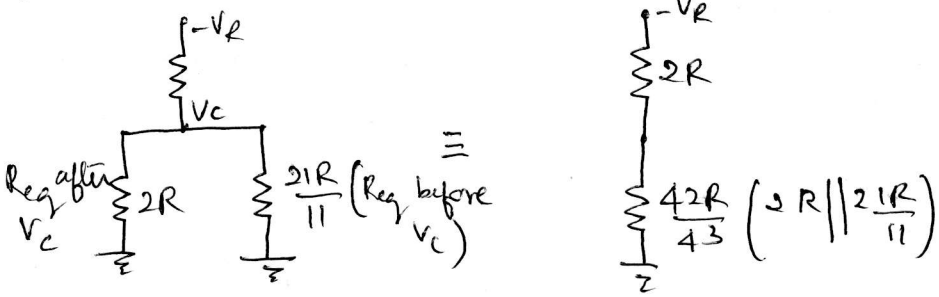
$$= -2\left(-\frac{V_R}{8}\right)$$

$$\boxed{V_o = \frac{2V_R}{8}}$$

Case (iii) :- 001



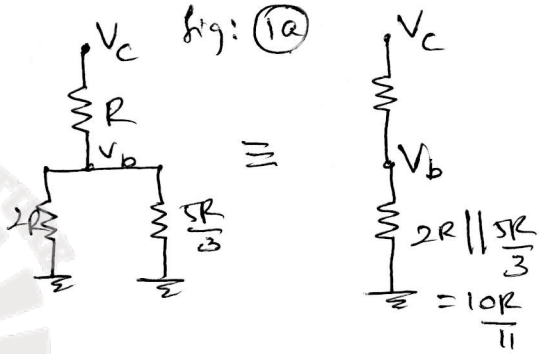
To determine Va



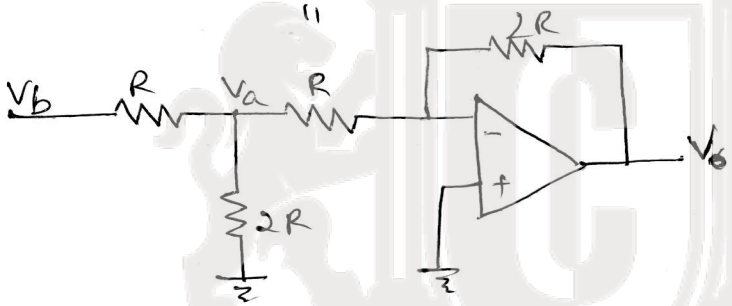
$$V_c = \frac{-V_R\left(\frac{42R}{43}\right)}{\frac{42R}{43}+2R} \quad (\because \text{vtg divider rule})$$

$$V_c = \frac{-V_R\left(\frac{42R}{43}\right)}{\frac{42R+86R}{43}} = \frac{-V_R\left(\frac{42R}{43}\right)}{\frac{128R}{64}} \Rightarrow \boxed{V_c = \frac{-21V_R}{64R}}$$

From fig: (1a) $V_b = \frac{V_c\left(\frac{10R}{11}\right)}{\frac{10R}{11}+R} = \frac{-\frac{21V_R}{64}\times\frac{10R}{11}}{\frac{10R}{11}+R}$



$$V_b = \frac{-\frac{21V_R}{64}\times\frac{10R}{11}}{\frac{21R}{11}} = \frac{-5V_R}{32}.$$



$$V_a = \frac{V_b\left(\frac{2R}{3}\right)}{\frac{2R}{3}+R} = \frac{-\frac{5V_R}{32}\times\frac{2R}{3}}{\frac{5R}{3}}$$

$$\therefore \boxed{V_a = \frac{-V_R}{16}}$$

now we have, $V_o = -2V_a$

$$= -2\left(\frac{-V_R}{16}\right)$$

$$\boxed{V_o = \frac{V_R}{8}}$$

similarly for $011 \rightarrow 010 + 001$

$$\frac{2V_R}{8} + \frac{V_R}{8} = \frac{3V_R}{8}$$

; $101 \rightarrow 100 + 001$; $110 \rightarrow 100 + 010$

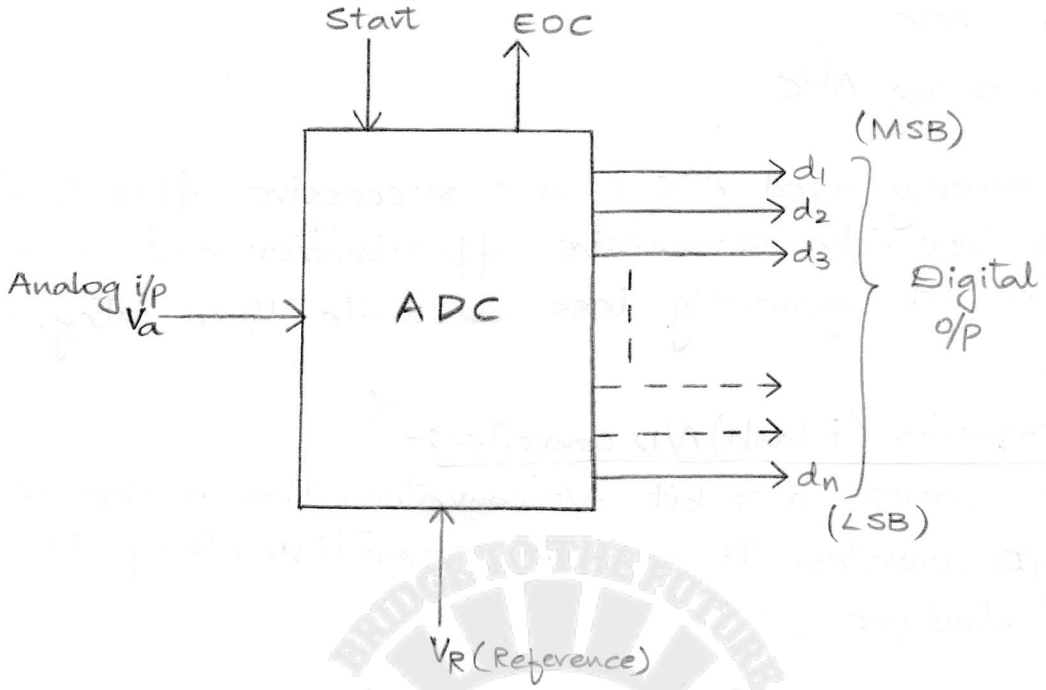
$\rightarrow \frac{5V_R}{8}$ $\rightarrow \frac{6V_R}{8}$

$111 \rightarrow 100 + 010 + 001$

$\rightarrow \frac{7V_R}{8}$

For these combinations we get V_o by super position theorem.

Analog to Digital Converters [ADC]



Functional diagram of ADC

The block schematic of ADC is shown in fig. It provides a function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1, d_2, ---- d_n$

The functional value of o/p D is

$$D = 2^{-1}d_1 + 2^{-2}d_2 + 2^{-3}d_3 + ---- + 2^{-n}d_n$$

ADC's are classified broadly into two groups according to their conversion technique

(i) Direct type ADC's

(ii) Integrating type ADC's

Direct type ADC's compare a given analog signal with the internally generated equivalent signal

Types of Direct type ADC

(i) Flash type ADC (or) Parallel comparator ADC ✗

(ii) Counter type ADC ✗

(iii) Tracking (or) Servo type ADC ✗

(iv) Successive approximation type ADC ✓

Integrating type ADC's perform conversion in an indirect manner by first changing the analog i/p signal to a linear function of time (or) frequency and then to a digital code

Types of Integrating type ADC

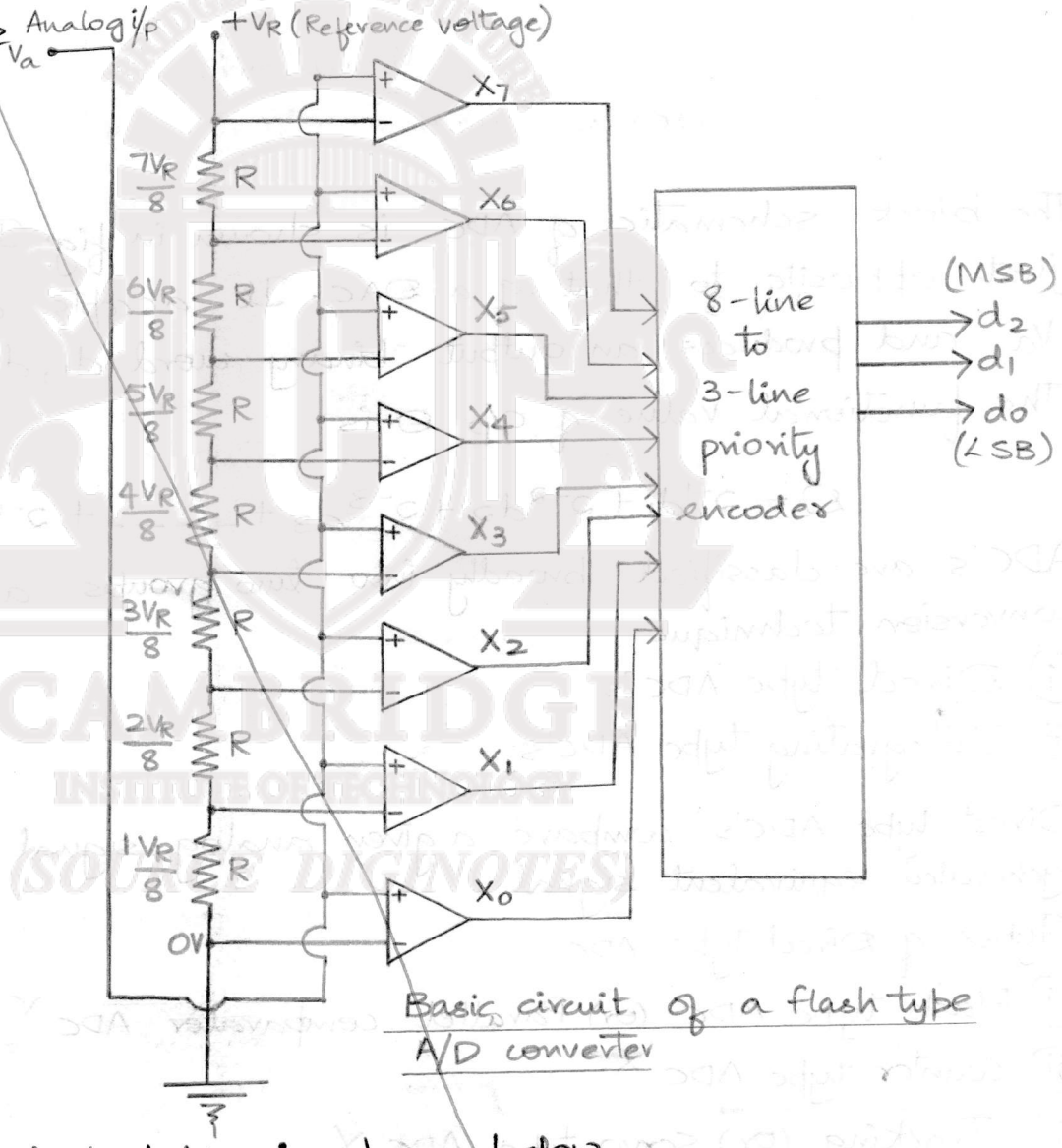
(i) Dual slope ADC

(ii) Charge balancing ADC

The most commonly used ADC's are successive approximation and the integrator type. The successive approximation and comparator type are faster but generally less accurate than integrating type converters.

(i) Parallel comparator (Flash) A/D converter :-

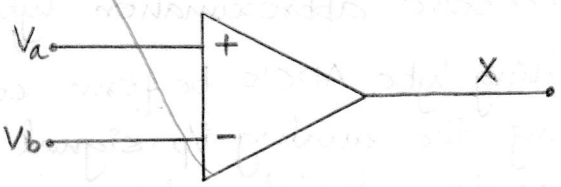
figure below shows a 3-bit A/D converter. This is the simplest possible A/D converter. It is at the same time, the faster and most expensive technique



Basic circuit of a flash type A/D converter

The comparator and its truth table is shown below

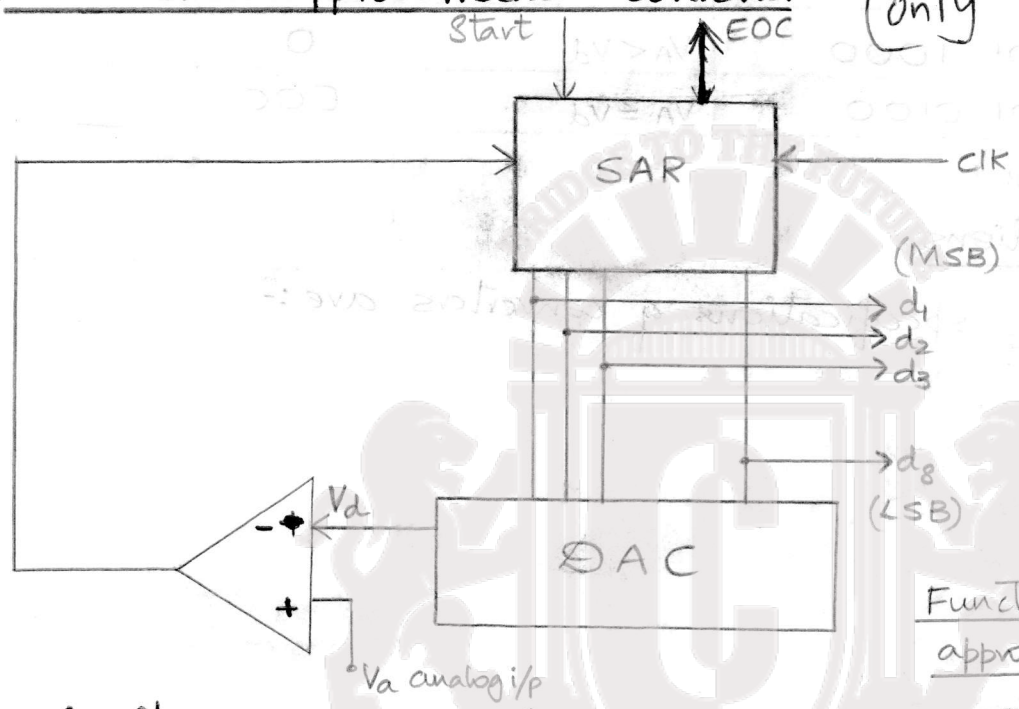
Voltage i/p	Logic o/p X
$V_a > V_d$	X=1
$V_a < V_d$	X=0
$V_a = V_d$	Previous value



When $V_d < V_A$, comparator o/p is high, counter acts as a up counter thus tracking for V_A. When $V_d > V_A$ the comparator o/p is low, counter acts as down counter, thus tracking for V_A. Here V_A can be varied & can be treated without Reseting each time.

The tracking ADC has the advantage of being simple. The disadvantage however is the time needed to stabilize as a new conversion value is directly proportional to the rate at which the analog signal changes.

(iv) Successive Approximation Converter [S.A.C] (Only S.A.C is kept in the syllabus)



Function diagram of successive approximation ADC

The circuit uses a SAR (Successive Approximation Register) to find the required value of each bit by trial and error

The circuit operates as follows:-

*) Set the SAR using start pulse. When the SAR is set the MSB $d_1 = 1$ with all other bits zero so that the trial code is 1000 0000

*) The output V_d of the DAC is now compared with analog input V_a

*) If V_a is greater than V_d, comparator o/p is 1. When comparator o/p is high the next MSB is made high and then checked.

*) If V_a is less than V_d, comparator o/p is 0. If comparator o/p is low the MSB bit that was made high earlier is reset to zero and the next bit is made high & then checked.

*) If V_a is equal to V_d, it is taken as End of conversion [EOC] command.

∴ comparator o/p = EOC

Succession approximation conversion sequence for a typical analog i/p

V_A (I/P)	SAR (O/P) V_d	difference b/w V_A & V_d	Comparator O/P
1101 0100	1000 0000	$V_A > V_d$	1
	1100 0000	$V_A > V_d$	1
	1110 0000	$V_A < V_d$	0
	1101 0000	$V_A > V_d$	1
	1101 1000	$V_A < V_d$	0
	1101 0100	$V_A = V_d$	EOC

DAC / ADC Specifications

The various important specifications of converters are :-

1. Resolution
2. Linearity
3. Accuracy
4. Monotonicity
5. Settling time
6. Stability

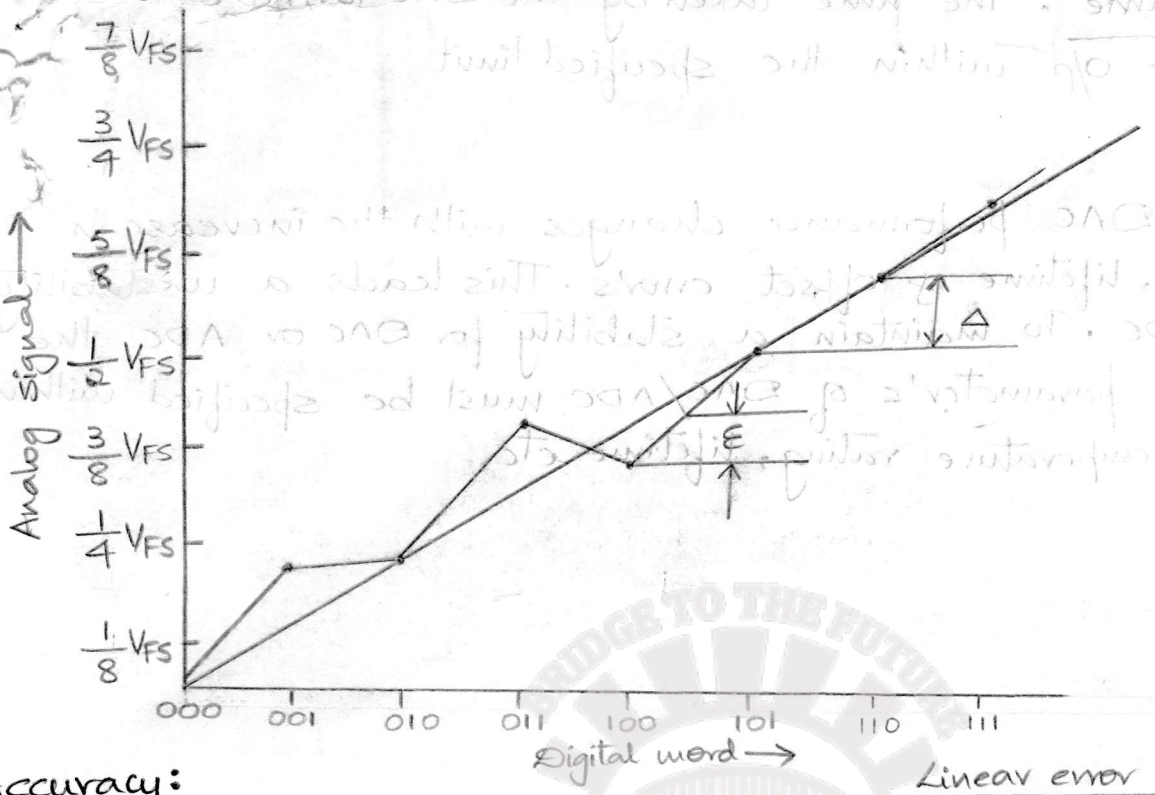
① **Resolution:** A small change in the voltage that can be produced in the o/p of DAC/ADC
It is the value of voltage available at LSB
Mathematically Resolution is given by

$$\boxed{\text{Resolution} = \frac{V_{FS}}{2^n - 1}}$$

② **Linearity:** Linearity is the parameter which measures the accuracy of the converter. This parameter gives how closeness is produced in the ideal DAC o/p.

The linearity error measures the deviation of the actual o/p from the fitted line & is given by ε/Δ. The error is usually expressed as a fraction of LSB increment or percentage of fullscale voltage.

A good converter exhibits a linearity error of less than $\pm(1/2)$ LSB



Linear error for 3 bit DAC

③ **Accuracy:**

There are 2 types

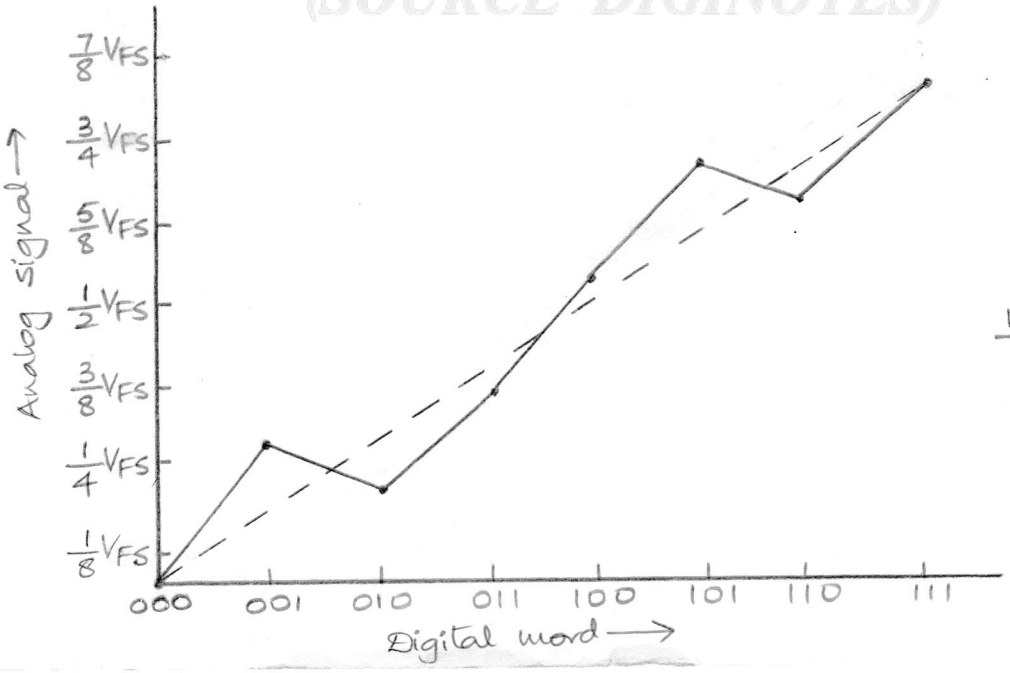
① Absolute Accuracy

② Relative Accuracy

① **Absolute Accuracy**: If the accuracy of the DAC/ADC is measured in the absense of gain, offset error's is known as absolute accuracy

② **Relative Accuracy**: If the accuracy of the DAC/ADC is measured in the presence of gain, offset error's is known as Relative accuracy

④ **Monotonicity**: If the o/p of actual DAC following the o/p of ideal DAC without maximum deviation then it is called Monotonicity otherwise there is a maximum deviation between the o/p's of actual DAC & ideal DAC known as Non-monotonicity



non-monotonic 3bit DAC

⑤ <u>Settling time</u> : The Time taken by the DAC (or) ADC to sett down the o/p within the specified limit

⑥ <u>Stability</u> : DAC performance changes with the increase in temperature, lifetime & offset error's. This leads a unstability for DAC/ADC. To maintain a stability for DAC or ADC the performance parameter's of DAC/ADC must be specified within maximum temperature rating, lifetime etc